DOCTORAL DISSERTATION IN
COMPUTER AND CONTROL ENGINEERING

RELIABILITY IN POWER ELECTRONICS AND POWER SYSTEMS

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PEIC
Power Electronics Innovation Center

Politecnico di Torino

GOAL

- Electronic devices used in modern power systems can be affected by faults
- It is important to detect the faulty devices by means of test methods
- Power electronics are increasingly used in safety-critical applications
- Currently, the effectiveness of test methods for power devices is qualitatively assessed without a fault model
- The absence of a precise fault model for power devices does not allow a systematic and exhaustive generation of the fault list for a power device
- The emerging IEEE P2427 standard proposes a first analog fault model

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- The emerging IEEE P2427 standard proposes a first analog fault model

- THESIS CONTRIBUTIONS:
  - A fault model for power devices is proposed
  - The fault model is used to assess the effectiveness of the power devices test procedures
  - The fault model is used to assess the effectiveness of thermal test procedures
  - The new fault model is used to study the impact of the device faults on cyber-physical systems

OUTLINE

1. INTRODUCTION
2. THE P2427 NEW FAULT MODEL: STATE OF THE ART
3. ASSESSING THE EFFECTIVENESS OF A TEST PROCEDURE FOR POWER DEVICES
4. ASSESSING THE EFFECTIVENESS OF A THERMAL TEST PROCEDURE FOR POWER DEVICES
5. ASSESSING POWER DEVICE FAULTS EFFECT IN COMPLEX CYBER-PHISICAL SYSTEMS
6. CONCLUSIONS

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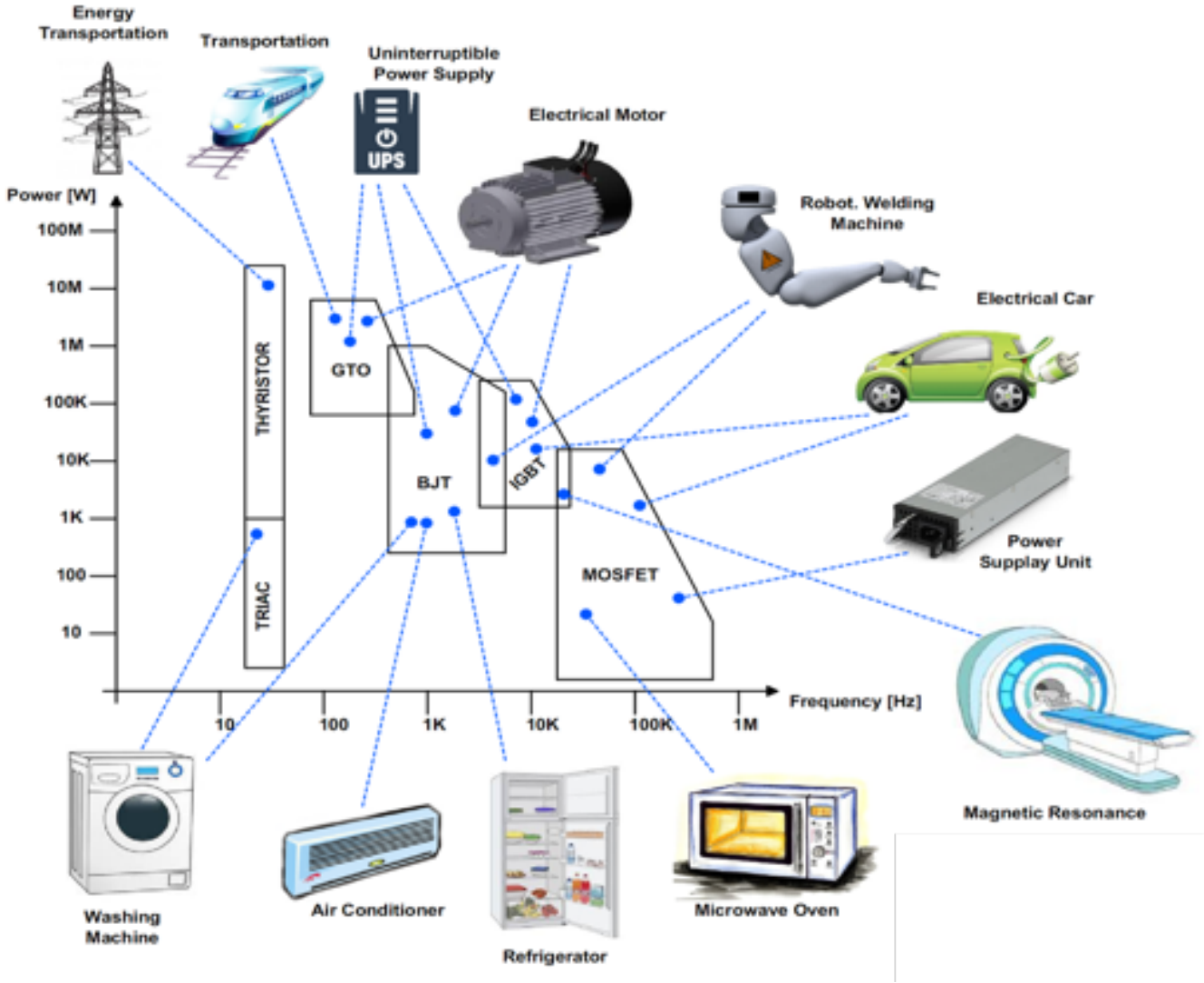
INTRODUCTION

- Power electronics is the application of the semiconductor devices to the high voltage and high current domain
- Different applications use power electronics and semiconductor power devices
- Some power applications are classified as safety-critical, such as
  - Energy transportation
  - People and goods transportation
  - Medical devices

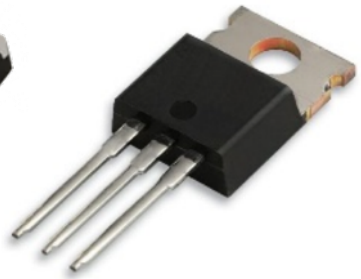


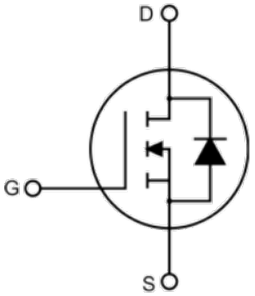
Examples of power devices

Diode

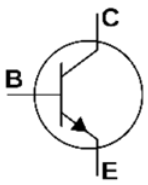
Power Diode

Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

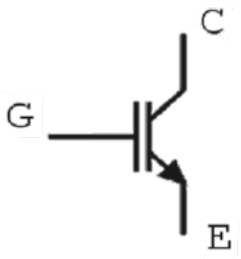




Bipolar Junction Transistor (BJT)



Insulated Gate Bipolar Transistors (IGBT)



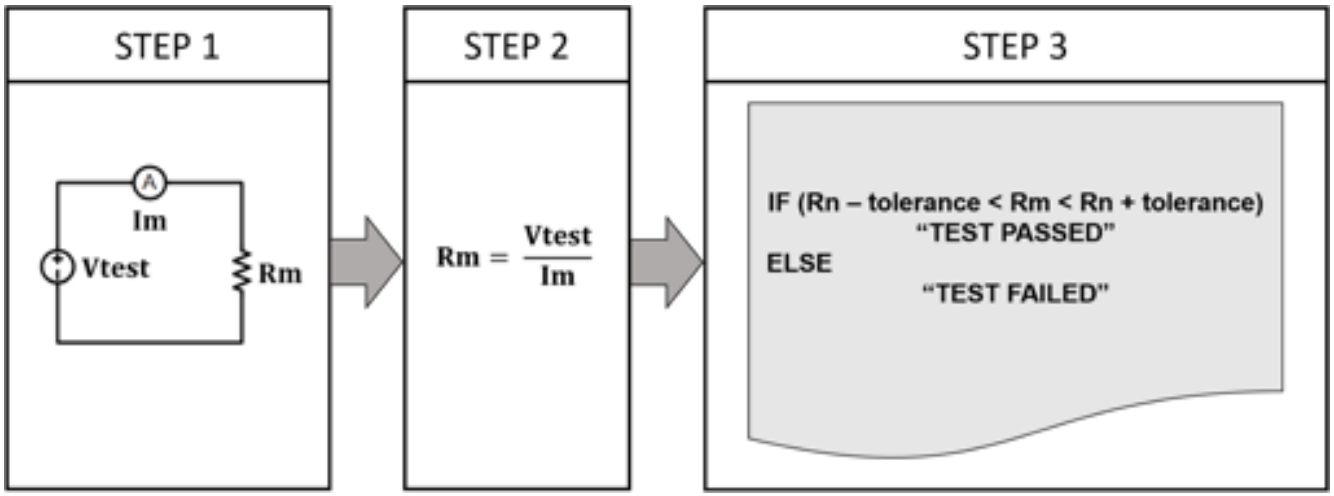
INTRODUCTION

- Testing plays a fundamental role, especially for safety-critical applications
- The role of test is to detect if something in the product has gone wrong
- In practice, the test checking the whole system, the different subsystems present in the product and the components that compose each subsystem
- In general, the test can be performed at the end-of-manufacturing and in-field
- The aim of the end-of-manufactoring test is to verify that the manufactured product correctly works after the assembly phases
- A test procedure is a sequence of steps that must be performed to execute a test

It is necessary to assess the effectiveness of the test procedure adopted

INTRODUCTION

- A test stimulus is an electrical signal (typically a voltage or a current) applied to the component under test for performing the test
- The response is measured on the component under test
- Typically, the response is a voltage or current signal measured on the component under test



Nominal resistance
Rn = 470 Ω ±5%

- In literature, there are numerous test procedures for other components and devices (Diode, MOSFET, IGBT, BJT, …)

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THE P2427 NEW FAULT MODEL

- In the last 10 years, different researchers have been involved in a working group with the aim of developing a standard for analog defect modelling
- The recent IEEE P2427 standard emerged from the research performed by the working group
- The final publication of the P2427 is expected at the end of 2022
- The first contribution provided by the P2427 standard is a set of definitions aimed at clearly and concisely indicating the quantitative information about the fault coverage of a test procedure

- IEEE P2427 defines a defect as *a permanent and unexpected change in a component parameter*
- The unexpected change is outside the manufacturing/design specifications of a circuit/component
- The IEEE P2427 defines
  - **the catastrophic fault model** (corresponding to hard faults)
  - **the parametric fault model** (corresponding to soft faults)

THE P2427 NEW FAULT MODEL

CATASTROPHIC FAULT MODEL

- The catastrophic faults are short circuits and/or open circuits in an electrical network
- An open circuit or a short circuit are modelled using electrical switches in the network
- Currently, the method of applying the fault model is not defined

PARAMETRIC FAULT MODEL

- Parametric faults are an alteration of a component parameter present in the circuit outside of its nominal range
- A parametric fault is defined as a change of a parameter in the behavioral/electrical model of a component
- Currently, the method of applying the fault model is not defined

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It is necessary to identify a rule to apply the fault models proposed in the IEEE P2427 standard to a circuit

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- A generic methodology to assess the effectiveness of a test procedure for a power device using the catastrophic fault model is proposed
- A methodology for generating the faults list of a power device is proposed
- The methodology is based on the equivalent electrical model of the Device Under Test (DUT)
- The equivalent electrical model of a device describes its behavior
- The fault simulation is performed resorting to an analog simulator (e.g. SPICE)
- Different test methods are considered (incoming inspection test, in-circuit test, functional test)

- Currently, the effectiveness of a test procedure is empirically assessed considering the experience of the engineers that developed the test, as discussed in:

[1] D. Bhatta, I. Mukhopadhyay, S. Natarajan, P. Goteti and Bin Xue, "Framework for analog test coverage," International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, pp. 468-475, March 2013

[2] M. G. Taul, X. Wang, P. Davari and F. Blaabjerg, "An Overview of Assessment Methods for Synchronization Stability of Grid-Connected Converters Under Severe Symmetrical Grid Faults," in IEEE Transactions on Power Electronics, vol. 34, no. 10, pp. 9655-9670, Oct. 2019

[3] S. Sunter, "Experiences with an industrial analog fault simulator and engineering intuition," 2015 IEEE 20th International Mixed-Signals Testing (IMST), Paris, pp. 1-5, August 2015

Incoming inspection test

In-circuit test

Functional test

Incoming inspection test

- It is performed on a single device
- The device under test is still disconnected from the Printed Circuit Board (PCB)
- Some test stimuli are applied to the device under test
- The device stimuli response is measured and compared with the expected one

In-circuit test

Functional test

Incoming inspection test

- It is performed on a single device
- The device under test is still disconnected from the Printed Circuit Board (PCB)
- Some test stimuli are applied to the device under test
- The device stimuli response is measured and compared with the expected one

In-circuit test

- The device under test is assembled on a PCB
- It is performed using an Automatic Test Equipment (ATE)
- The ATE directly contact the device under test and applies some test stimuli
- The ATE measures the stimuli response on the device under test
- Guard probes may be required

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- Guard probes may be required

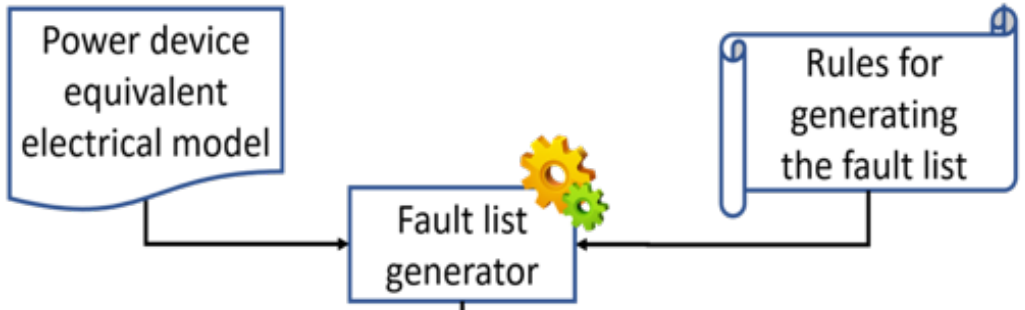
Functional test

- The test is performed with respect to its design specifications
- Only the input/output PCB interfaces are used
- Some functional test stimuli are applied to the PCB input port
- In steady state, the stimuli-response are measured on some PCB output port

Analog fault simulation flow

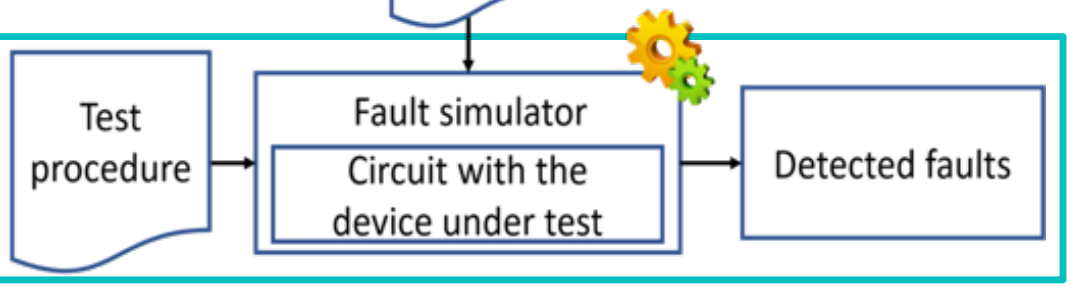
Step1

- In the first step, the fault list for the power device is generated



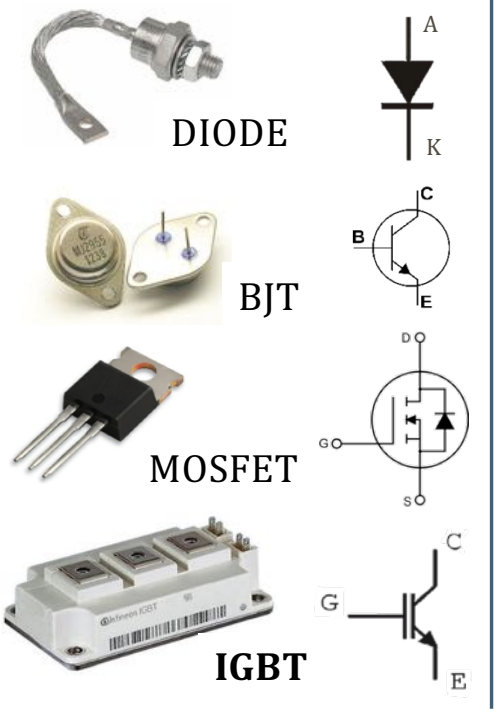
Step2

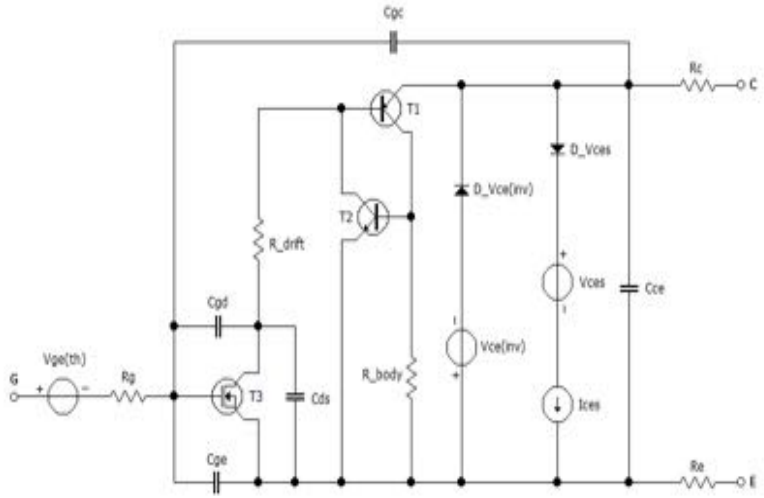
- In the second step, the fault simulation is performed
- A single fault is injected at time



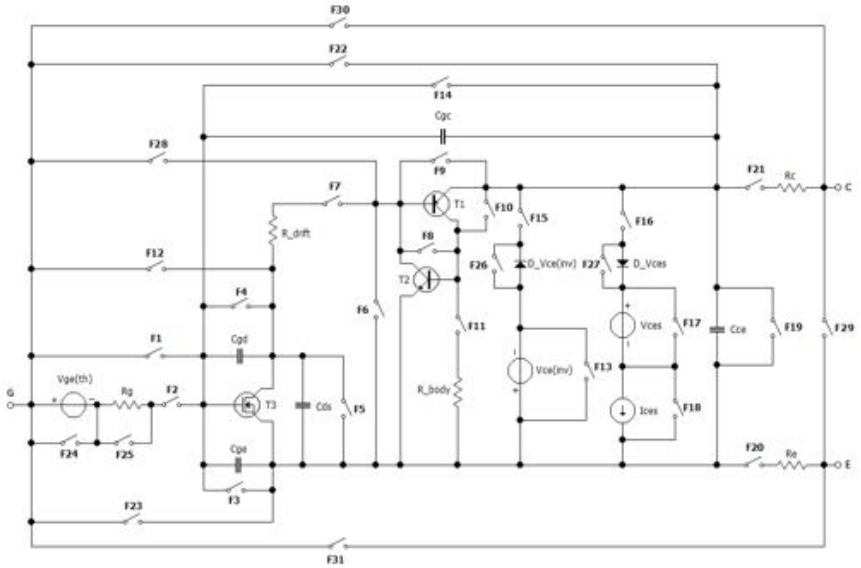
Step 1

Power device → Model → Equivalent electrical model → Fault list generation → Catastrophic faults in the equivalent electrical model





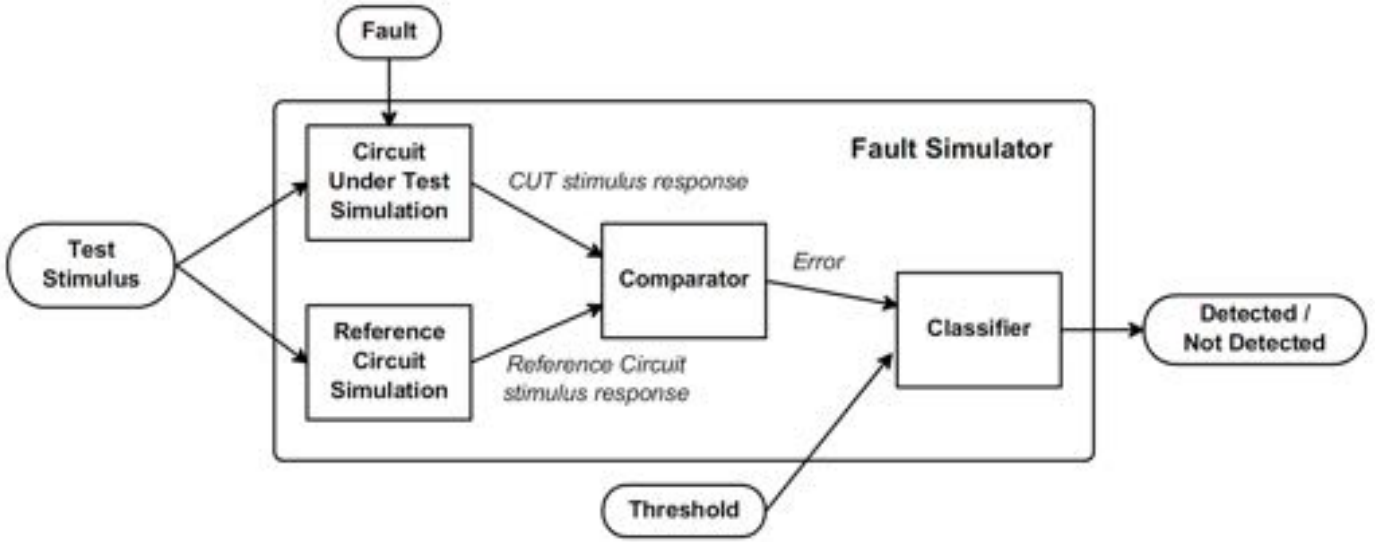
IGBT equivalent electrical model



31 catastrophic faults in the IGBT equivalent electrical model

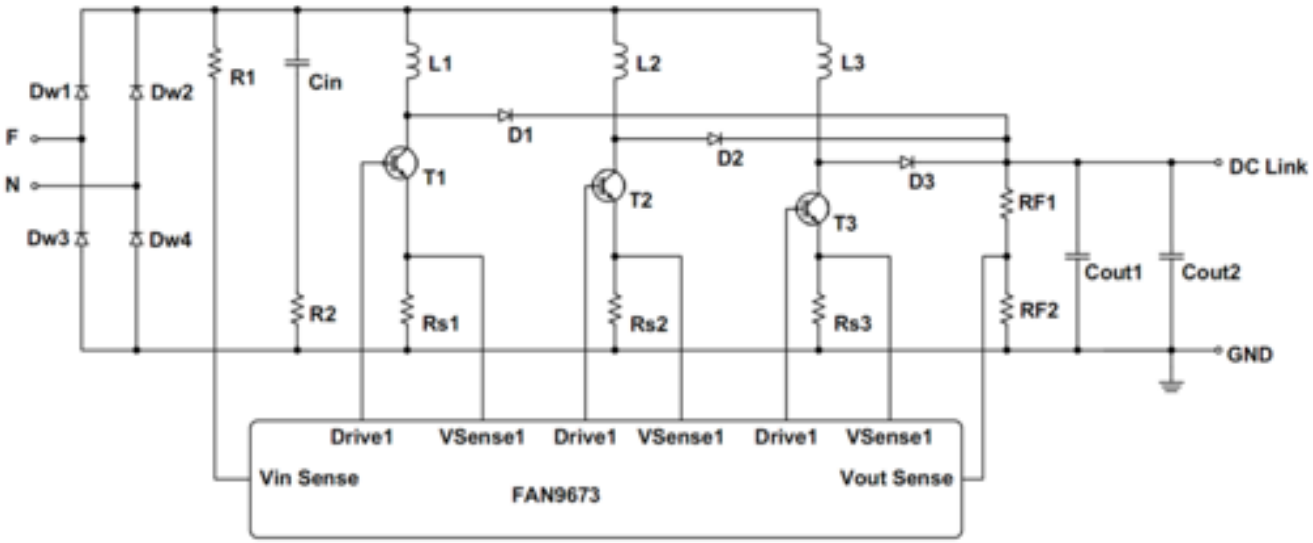
- Analog fault simulation flow
- A single fault is considered
- The test stimuli are applied to a reference circuit and to a circuit under test
- The stimulus responses are compared for generating an error signal
- If the error signal exceeds a given threshold, the injected fault is classified as detected (DT)
- A FC figure is computed

Step2



$$FC = \frac{\#DT}{\#tot.faults}$$

- A high-voltage Power Supply Unit (PSU) for a three-phase motor control system is considered
- The PSU has in input the grid voltage
- The PSU supplies a DC 400 V ±7 V in output with a 12 A of maximum current
- The high-voltage PSU consists of three boost cells driven by the FAN9673 analog controller
- STTH12S06 is the diode under test
- STGF19NC60 is the IGBT under test



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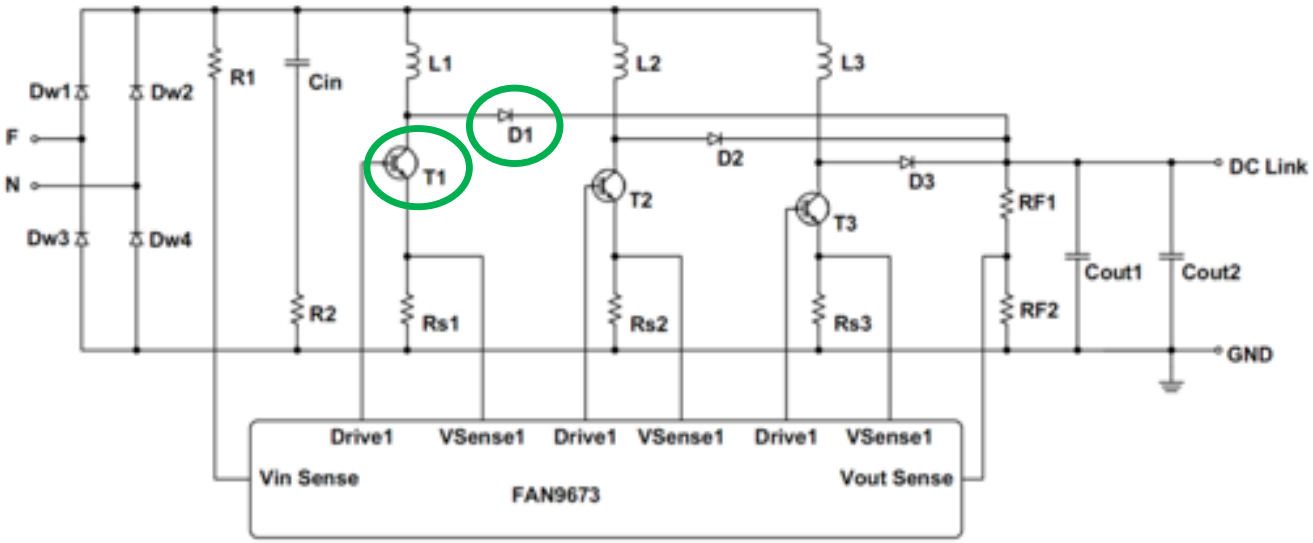

DUT	# Catastrophic faults
STTH12S06 diode	4
STGF19NC60 IGBT	31

- Five different test methods are considered

	DIODE		**IGBT**	
	# Test stimuli applied	FC	# Test stimuli applied	FC
Incoming inspection test	2 test steps	4 out of 4	8 test steps	31 out of 31
In-circuit test	1 test step	1 out of 4	6 test steps	25 out of 31
Functional test	4 test step	4 out of 4	4 test step	15 out of 31
Functional timely enhanced test	4 test step	4 out of 4	4 test step	20 out of 31
Functional observability enhanced test	4 test step	4 out of 4	4 test step	24 out of 31

- Incoming inspection test detects all possible catastrophic faults
- However, the power device is not yet assembled on the PCB

	DIODE		IGBT	
	# Test stimuli applied	FC	# Test stimuli applied	FC
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Functional observability enhanced test	4 test step	4 out of 4	4 test step	24 out of 31

Functional test is enough to fully test the diode assembled on the PCB

	DIODE		IGBT	
	# Test stimuli applied	FC	# Test stimuli applied	FC
Incoming inspection test	2 test steps	4 out of 4	8 test steps	31 out of 31
In-circuit test	1 test step	1 out of 4	6 test steps	25 out of 31
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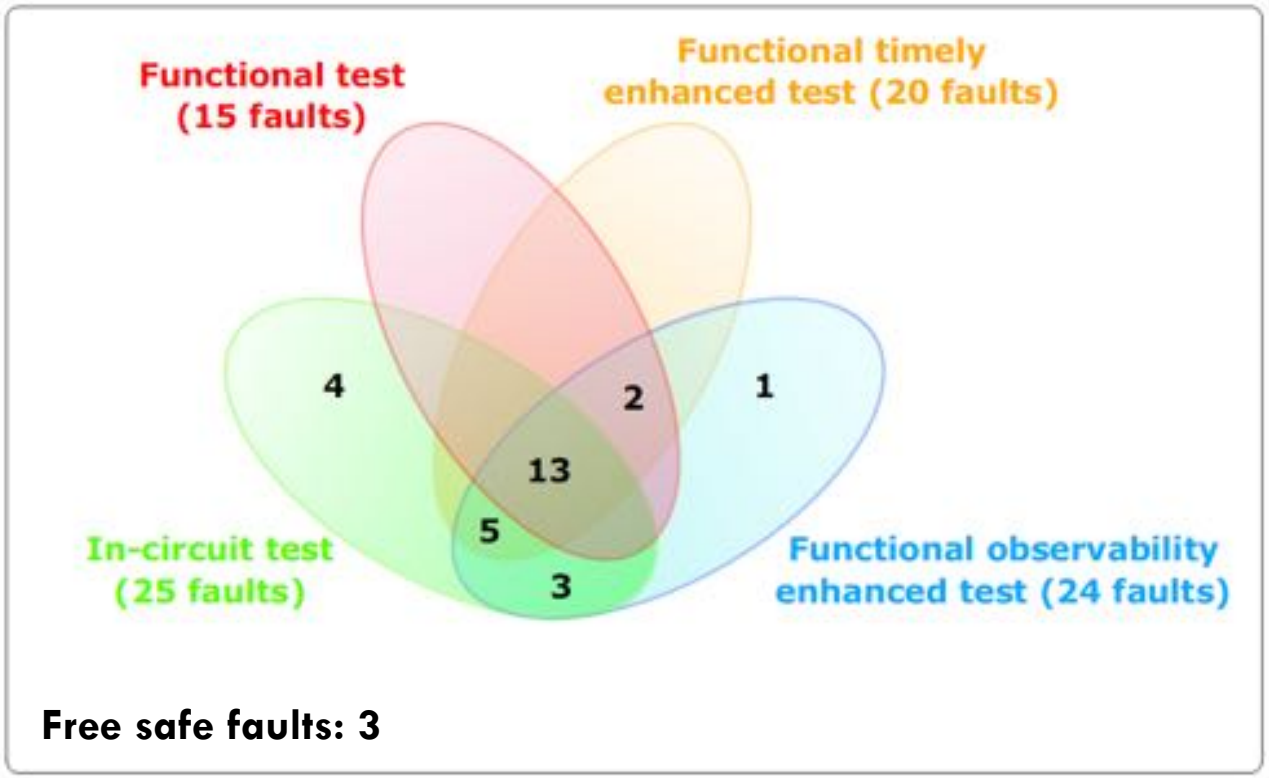
It is necessary to identify an optimal set of tests for the IGBT

- The graph shows the number of faults detected by each test method considered
- Some faults are detected only by a test methods
- Some faults are detected by different test methods
- *Functional test* and *functional timely enhanced functional test* methods do not introduce any contribution to the final FC
- *In-circuit test* and *functional observability enhanced test* methods combined allow to detect **28 faults out of 31**
- The remaining 3 undetected faults are safe

IGBT DEVICE FC



Free safe faults: 3

- A methodology for assessing the effectiveness of a test method for a power device has been proposed
- The proposed methodology is able to automatically and systematically generate the fault list
- The rules proposed for generating the fault list are general and independent of the device under test
- A possible approach for performing an analog fault simulation is proposed
- The proposed analog fault simulation approach can be applied to different test methods
- A FC figure for each test method is computed
- The proposed approach allows identifying the faults that are never detected by any test method
- The proposed approach allows identifying the best set of test methods

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- The temperature management is a non-secondary aspect in the design of power circuits and systems
- Junction temperature (Tj) has a significant impact on the semiconductor device behavior
- Moreover, high Tj accelerates the failure mechanisms of power devices and reduces their lifetime
- Typically, a heatsink is used for dissipating the heat produced by the power device
- An incorrect heatsink assembly may cause an unacceptable Tj increase inside the power device
- A methodology for testing the correct heatsink assembling on a power device is proposed
- Moreover, a methodology for assessing the effectiveness of a thermal test method is proposed

- Currently, the heatsink test is in most cases performed using manual or automatic optical inspections or resorting to the x-ray technology

- Furthermore, the effectiveness of these thermal test methods is assessed qualitatively without considering a fault model

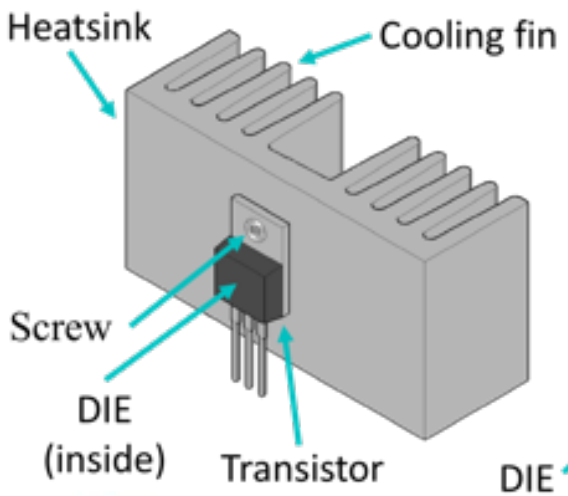
[4] L. Zhu-Mao, L. Qing, J. Tao, L. Yong-Xin, H. Yu and B. Yang, "Research on Thermal Fault Detection Technology of Power Equipment based on Infrared Image Analysis," 2018 IEEE 3rd Advanced Information Technology, Electronic and Automation Control Conference (IAEAC), Chongqing, 2018, pp. 2567-2571

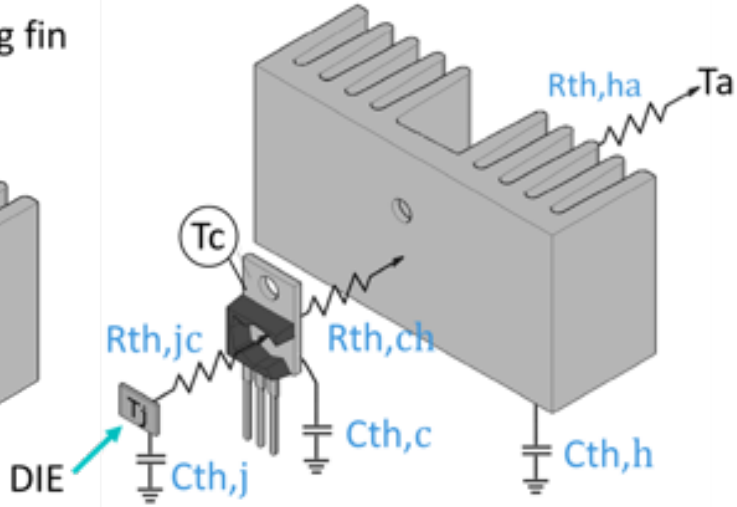
[5] F. Stella, G. Pellegrino, E. Armando and D. Daprà, "Online Junction Temperature Estimation of SiC Power MOSFETs Through On-State Voltage Mapping," in IEEE Transactions on Industry Applications, vol. 54, no. 4, pp. 3453-3462, July-Aug. 2018

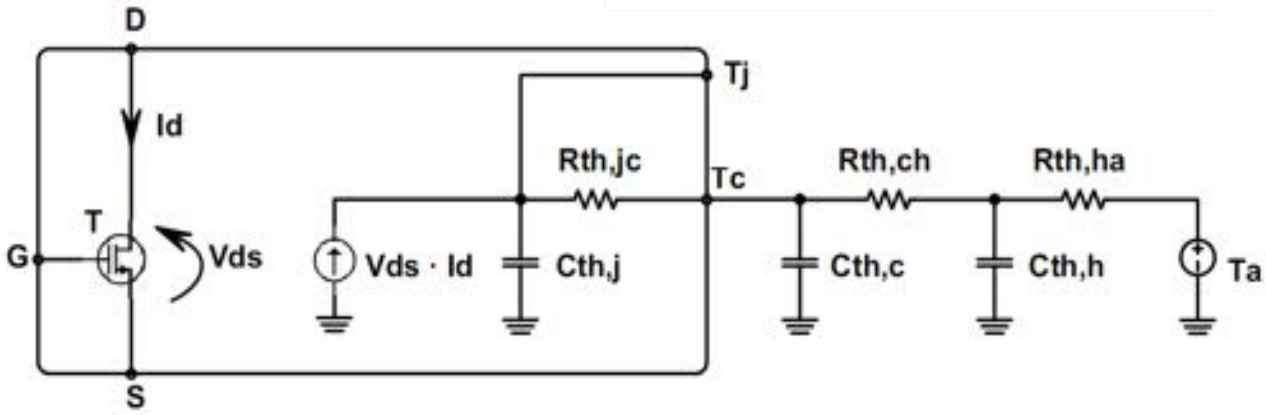
[6] A. P. Ferreira, D. Mosse and J. C. Oh, "Thermal Faults Modeling Using a RC Model with an Application to Web Farms," 19th Euromicro Conference on Real-Time Systems (ECRTS'07), Pisa, 2007, pp. 113-124

Thermal model of the dissipation system

- The power device is in steady state
- An electrical network models the thermal dissipation system
- A current generator models the heat produced by the power device
- A voltage generator models the ambient temperature
- Tj is measured on the current generator
- Rth,ch value depends on the heatsink assembly on the power device







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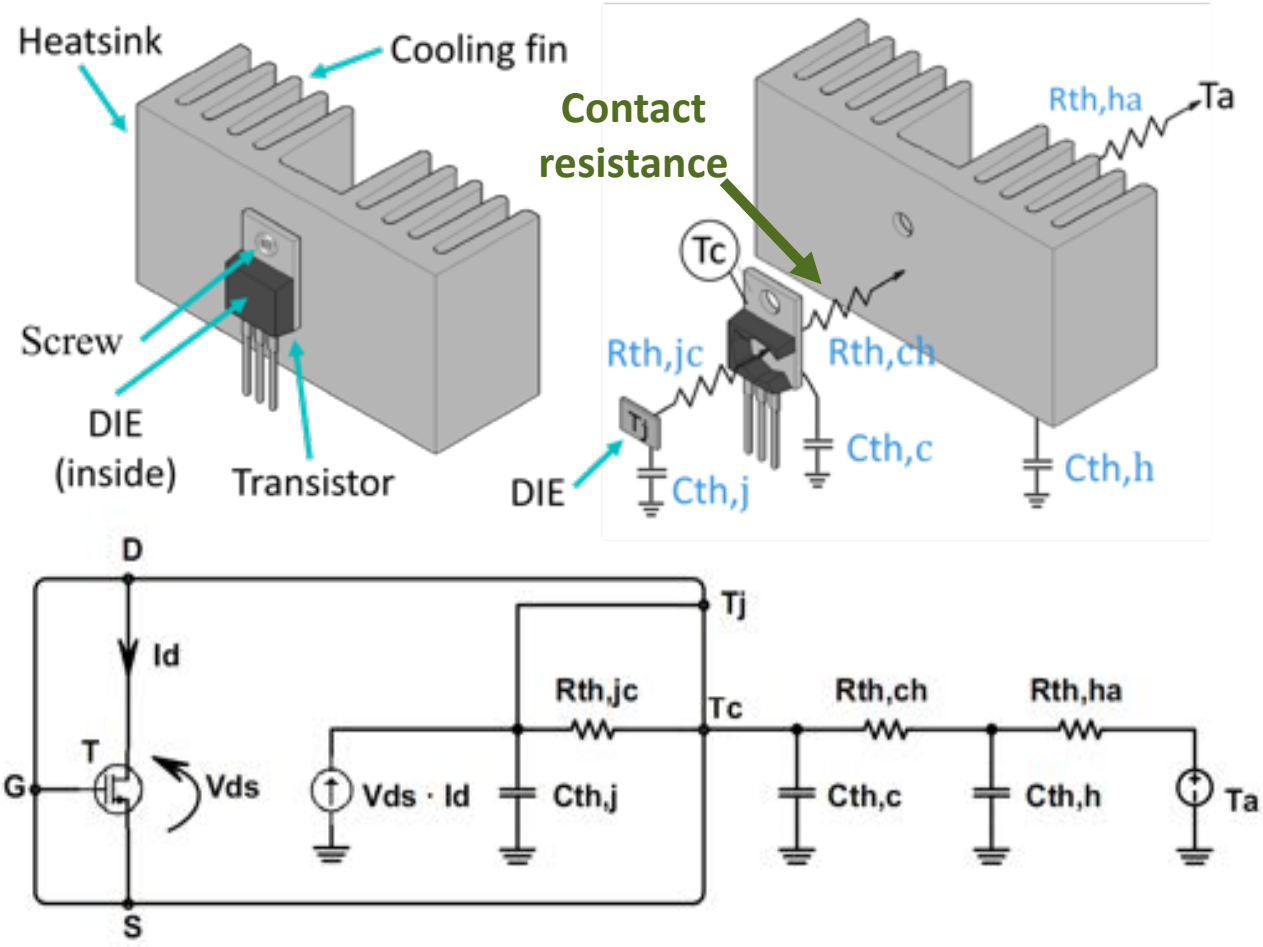
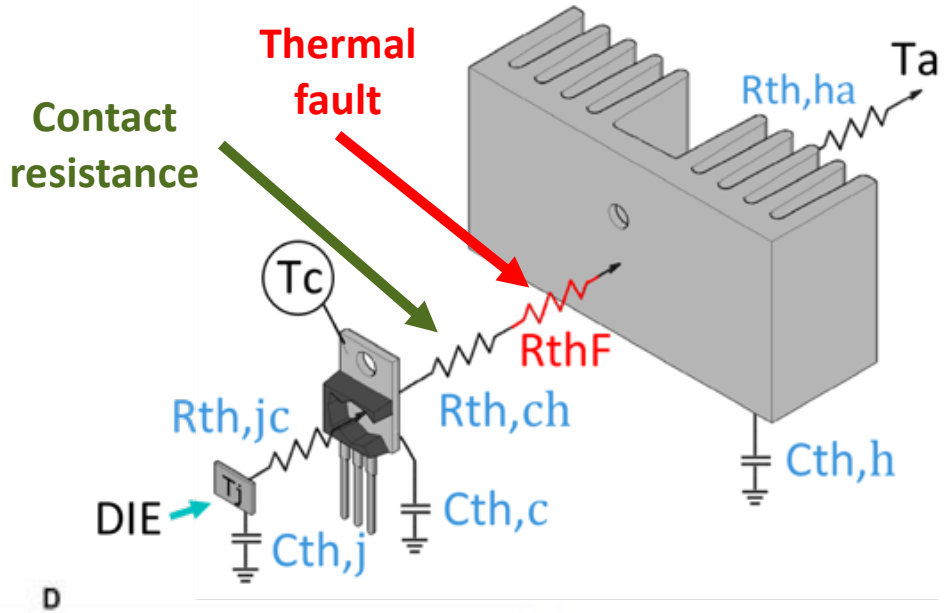
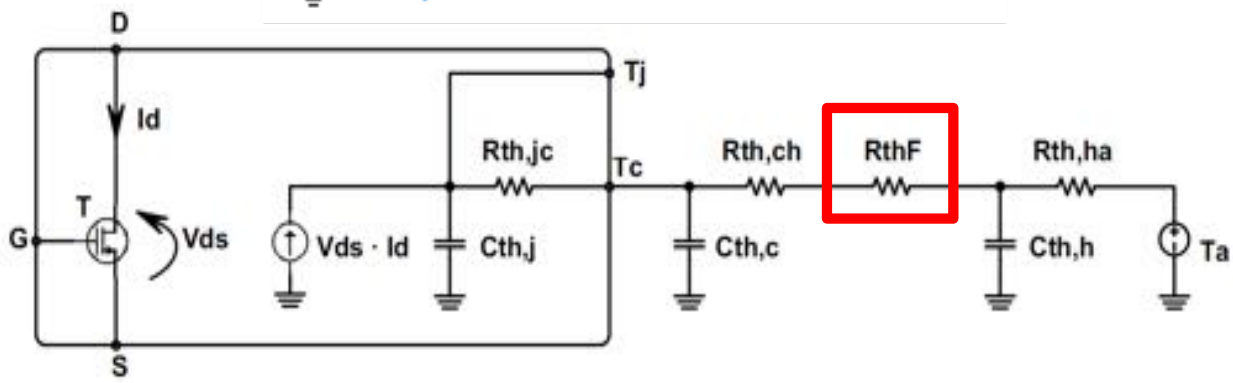
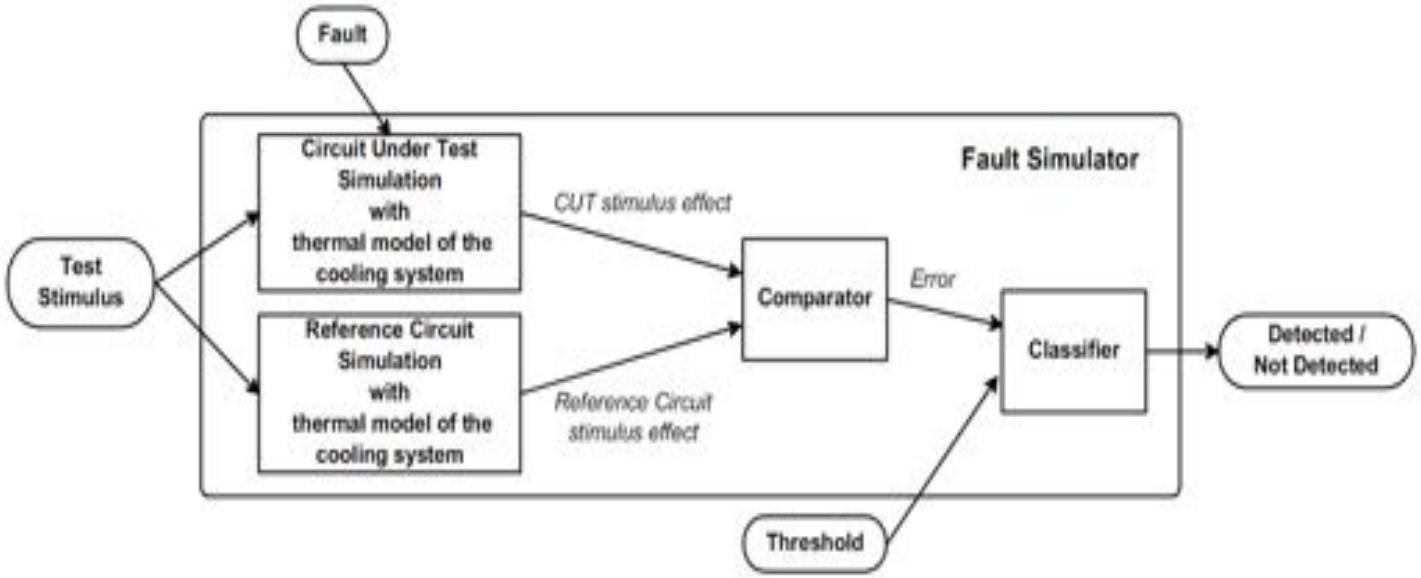


- A thermal fault resistance (RthF) is added in the thermal model
- RthF is added in the model in series to the contact resistance (Rth,ch)
- RthF identifies a further heat propagation obstacle due to an incorrect heatsink assembly
- With reference to the IEEE P2427 standard, RthF can be considered as parametric fault
- The value of RthF is identified in order to maximize the junction temperature of the power device



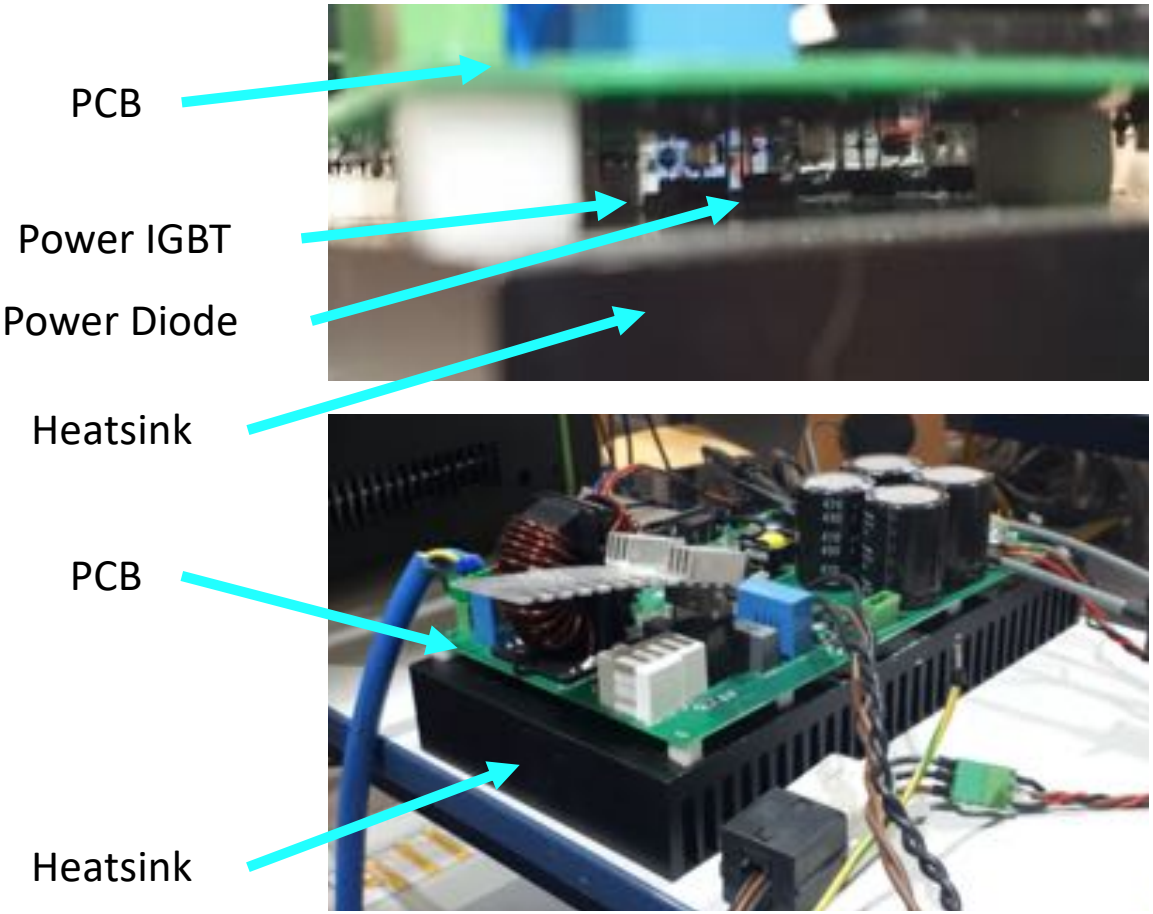


- Thermal fault simulation flow
- The single fault scenario is considered
- The test stimuli are applied to a reference circuit and to a circuit under test
- The stimulus-respons are compared for generating an error signal
- If the error signal exceeds a threshold, the injected fault is classified as detected (DT)



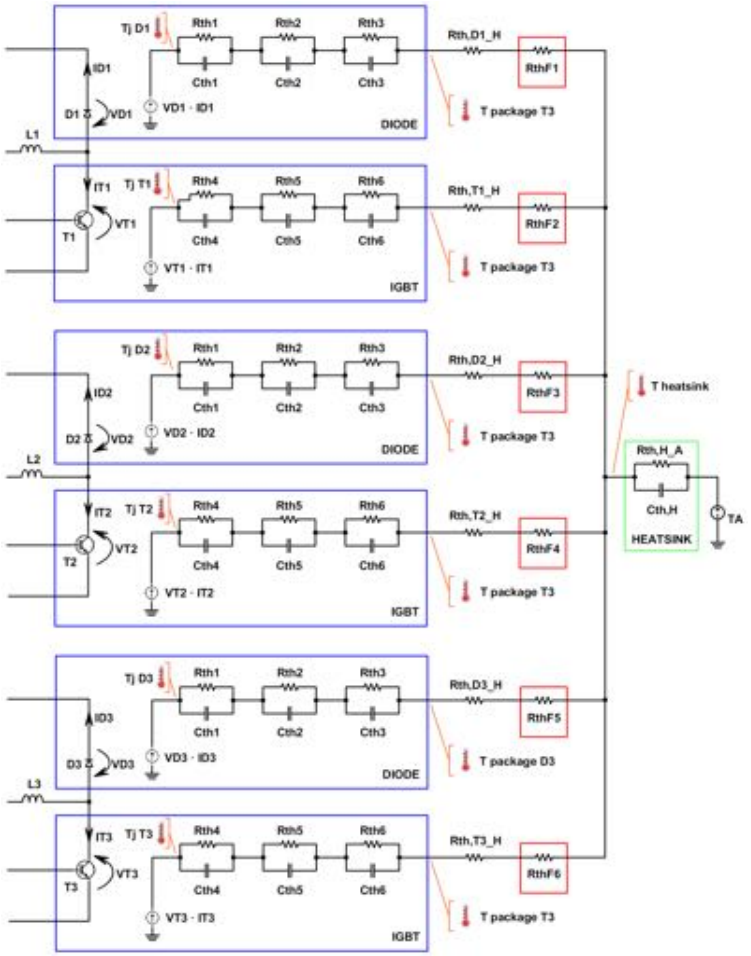
$$FC = \frac{\#DT}{\#tot.faults}$$

- A high-voltage Power Supply Unit (PSU) for a three-phase motor control system is considered
- 6 power devices share the same heatsink (3 diodes and 3 IGBTs)
- 6 thermal faults resistances are considered in the thermal model
- The heatsink on the STTH12S06 diodes and on the STGF19NC60 IGBTs is considered



- A thermal model for the high-voltage PSU heatsink is used
- The thermal model of the Infineon STTH12S06 diode is delivered by the manufacturer
- The thermal model of the Infineon STGF19NC60 IGBT is delivered by the manufacturer
- The STTH12S06 diode Tjmax is 150 °C
- The STGF19NC60 IGBT Tjmax is 100 °C

Thermal faults	Value
RthF1, RthF3, RthF5	16.7 °C/W
RthF2, RthF4, RthF6	10.3 °C/W



ASSESSING THE EFFECTIVENESS OF A THERMAL TEST PROCEDURE FOR POWER DEVICES

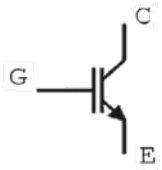
	Vf	Id	Tj	Rthja	Tpackage	Theatsink
Fault-free	1.46 V	0.5 A	31.2 °C	8.5 °C/W	27.2 °C	25.4 °C
With fault	1.45 V	0.5 A	31.3 °C	8.7 °C/W	27.7 °C	25.5 °C

Thermal in-circuit test diode device

	Vf	Id	Tj	Rthja	Tpackage	Theatsink
Fault-free	1.3 V	5.4 A	82.9 °C	8.2 °C/W	38.4 °C	28.2 °C
With fault	1.1 V	5.4 A	151.1 °C	17.3 °C/W	95.6 °C	28.4 °C

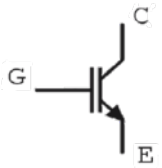
Thermal functional test diode device

	Vce	Ic	Tj	Rthja	Tpackage	Theatsink
Fault-free	1.36 V	1.04 A	62.1 °C	22 °C/W	42.3 °C	26.1 °C
With fault	1.53 V	1.27 A	110.8 °C	47 °C/W	91.7 °C	25.5 °C



Thermal in-circuit test IGBT device

	Vce	Ic	Tj	Rthja	Tpackage	Theatsink
Fault-free	0.75 V	0,91 A	71.1 °C	11.4 °C/W	33.7 °C	28.3 °C
With fault	1.12 V	0.94 A	151.2 °C	20.9 °C/W	86.3 °C	28.5 °C



Thermal functional test IGBT device

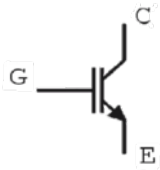
	Vf	Id	Tj	Rthja	Tpackage	Theatsink
Fault-free	1.46 V	0.5 A	31.2 °C	8.5 °C/W	27.2 °C	25.4 °C
With fault	1.45 V	0.5 A	31.3 °C	8.7 °C/W	27.7 °C	25.5 °C

Thermal in-circuit test diode device

	Vf	Id	Tj	Rthja	Tpackage	Theatsink
Fault-free	1.3 V	5.4 A	82.9 °C	8.2 °C/W	38.4 °C	28.2 °C
With fault	1.1 V	5.4 A	151.1 °C	17.3 °C/W	95.6 °C	28.4 °C

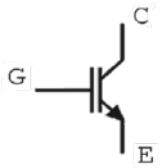
Thermal functional test diode device

	Vce	Ic	Tj	Rthja	Tpackage	Theatsink
Fault-free	1.36 V	1.04 A	62.1 °C	22 °C/W	42.3 °C	26.1 °C
With fault	1.53 V	1.27 A	110.8 °C	47 °C/W	91.7 °C	25.5 °C



Thermal in-circuit test IGBT device

	Vce	Ic	Tj	Rthja	Tpackage	Theatsink
Fault-free	0.75 V	0,91 A	71.1 °C	11.4 °C/W	33.7 °C	28.3 °C
With fault	1.12 V	0.94 A	151.2 °C	20.9 °C/W	86.3 °C	28.5 °C



Thermal functional test IGBT device

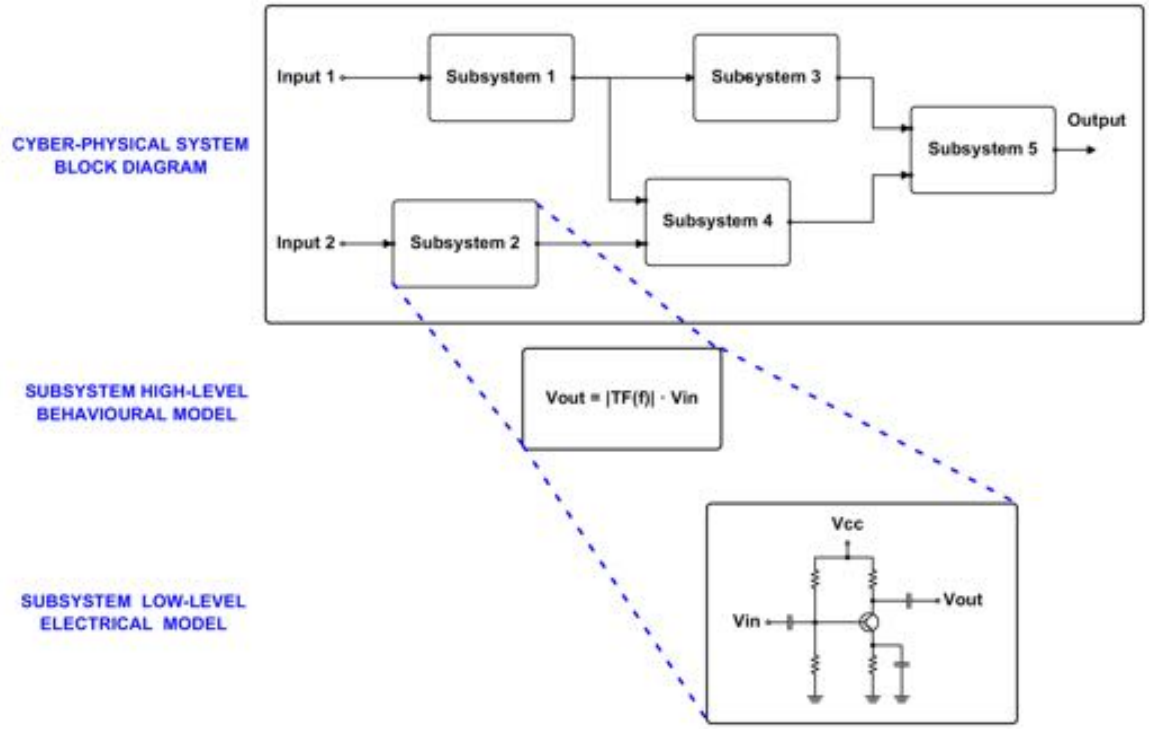
- A methodology for performing a thermal in-circuit test and a functional thermal test of the heatsinks assembly on power devices is proposed
- The proposed methodology does not require thermal measurements
- A methodology for generating the thermal fault list in the thermal model of a cooling system is proposed
- The effectiveness of the thermal in-circuit test and functional thermal test is assessed using the thermal model of the cooling systems
- The effectiveness of the thermal in-circuit test and functional thermal test procedure was also evaluated experimentally by intentionally assembling the heatsink in different incorrect configurations

OUTLINE

1. INTRODUCTION
2. THE P2427 NEW FAULT MODEL: STATE OF THE ART
3. ASSESSING THE EFFECTIVENESS OF A TEST PROCEDURE FOR POWER DEVICES
4. ASSESSING THE EFFECTIVENESS OF A THERMAL TEST PROCEDURE FOR POWER DEVICES
5. **ASSESSING POWER DEVICE FAULTS EFFECT IN COMPLEX CYBER-PHISICAL SYSTEMS**
6. CONCLUSIONS

- Different international standards require analyzing the fault impact on the cyber-physical system behavior, especially for safety-critical ones
- A possible approach to perform the Failure Mode, Effects, and Criticality Analysis (FMECA) analysis considering the new faults inside the power device is proposed
- The proposed approach exploits the state of the art of modern Electronic Design Automation (EDA) tools for performing the FMECA analysis
- The FMECA approach allows identifying the critical faults present in a cyber-physical system, i.e., the faults that bring the system in a potentially harmful unsafe state
- The approach proposed exploits a multilevel simulator using behavioral model and electrical model of the subsystems present in the cyber-physical system
- The fault effect is propagated through the different subsystems of the cyber-physical system for studying the behavior of the system affected by a fault

- Cyber-physical systems are composed of different dedicated subsystems that perform a specific task
- The different subsystems are interconnected creating a high-level block diagram of the overall system
- The behavioural model is characterized by a set of equations that describe the relationships between its inputs and outputs
- The circuit diagram is the electrical low-level model of an electrical subsystem



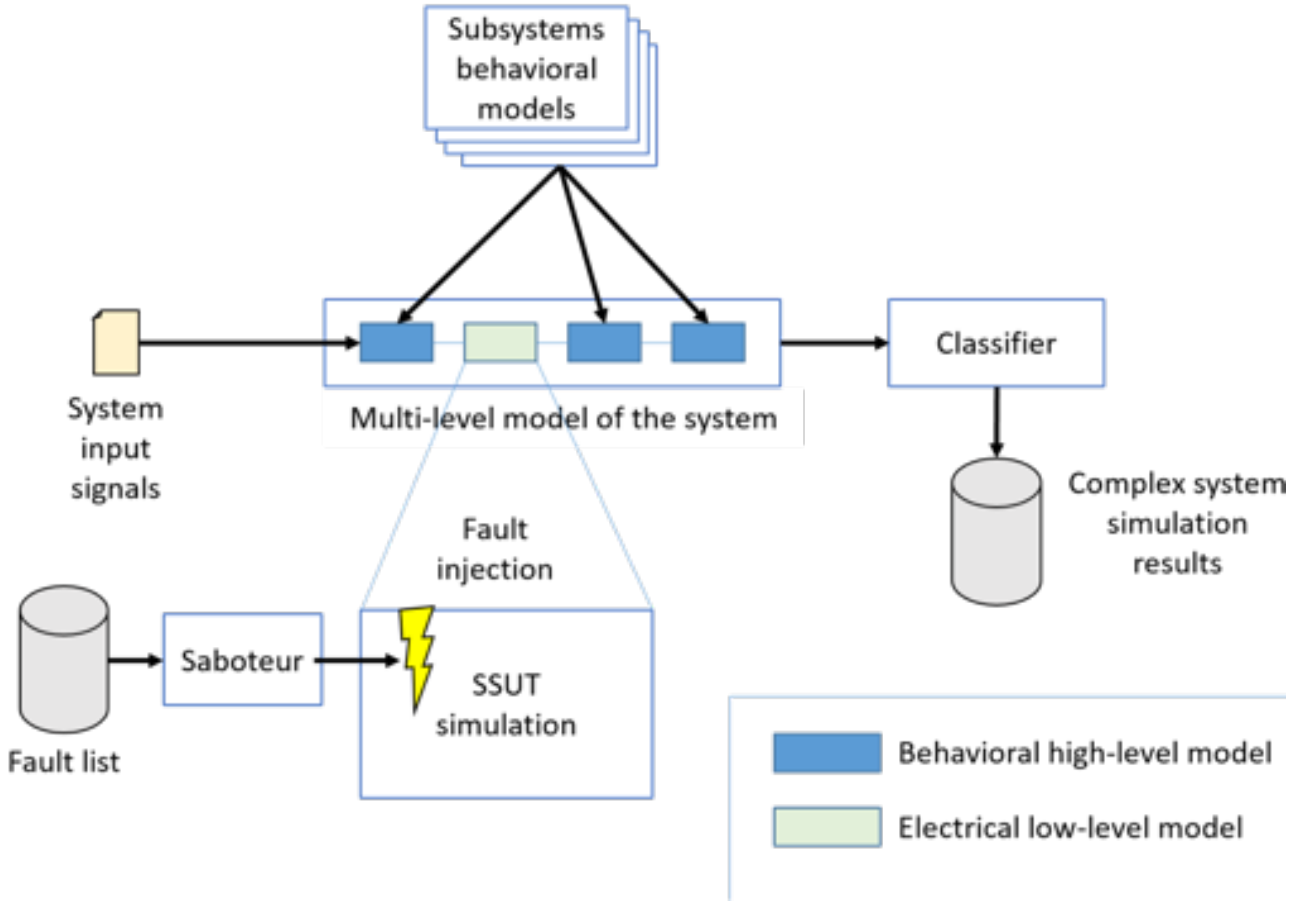
- With respect to other works proposed in literature, the approach proposed for performing the FMECA analysis is more accurate and complete

[7] S. Peyghami, P. Davari, M. F-Firuzabad and F. Blaabjerg, "Failure Mode, Effects and Criticality Analysis (FMECA) in Power Electronic based Power Systems," 2019, 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), 2019, pp. P.1-P.9

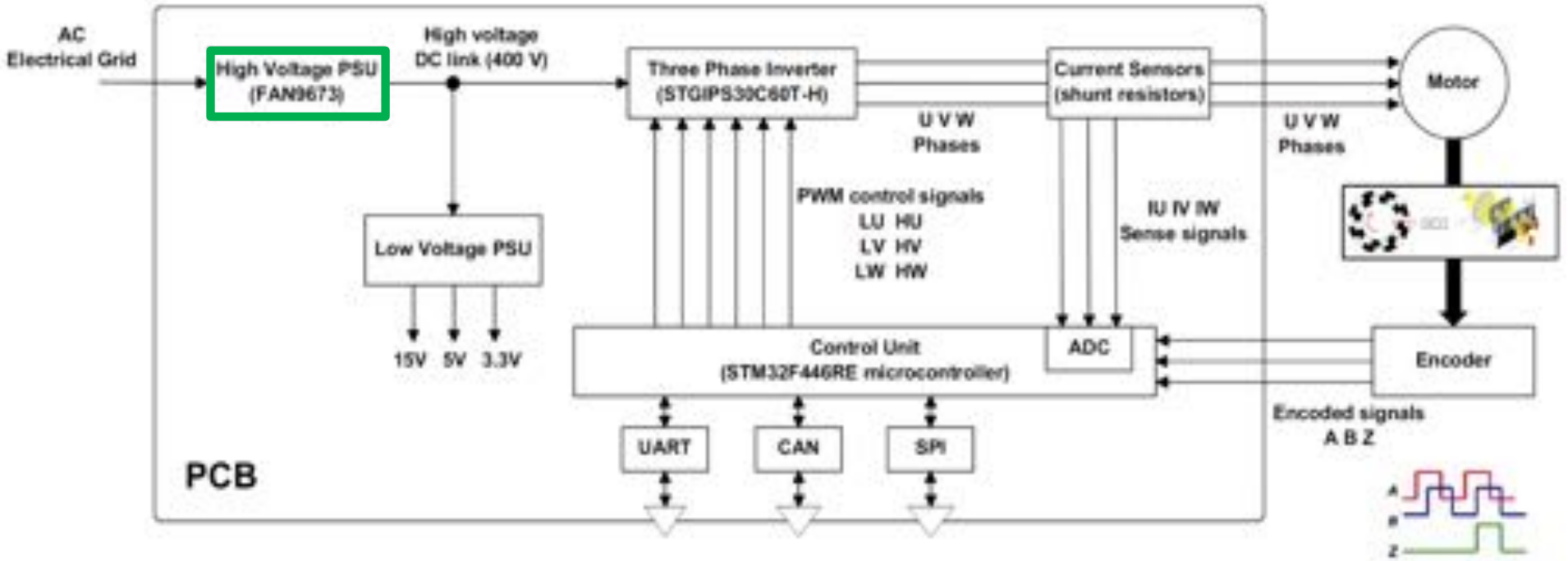
[8] A. Sastry et al., "Failure modes and effect analysis of module level power electronics," 2015, IEEE 42nd Photovoltaic Specialist Conference (PVSC), 2015, pp. 1-3

[9] J. Sini, M. D'Auria and M. Violante, "Towards Vehicle-Level Simulator Aided Failure Mode, Effect, and Diagnostic Analysis of Automotive Power Electronics Items," 2020 IEEE Latin-American Test Symposium (LATS), 2020, pp. 1-6

- A multilevel simulator is used
- The SubSystem Under Test (SSUT) is modelled at electrical level, while the other subsystems are modelled at behavioral level
- The faults are injected in the SSUT power device
- The cyber-physical system behaviour is compared to the expected one for classifying the injected fault as critical or not-critical



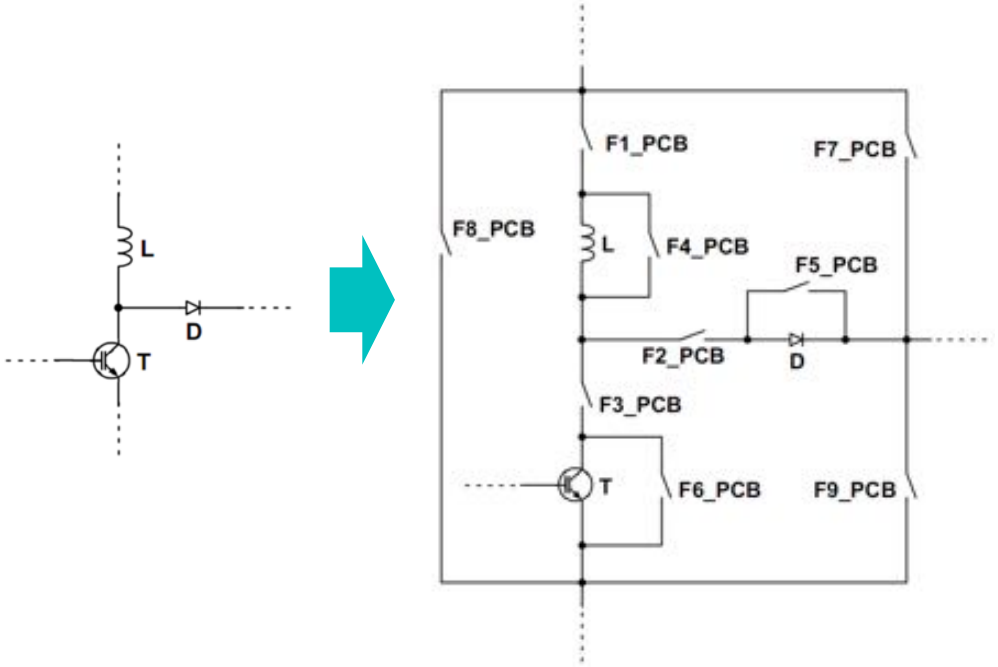
- The considered cyber-physical system is the control system of a three-phase electric motor
- The SubSystem Under Test is the high-voltage Power Supply Unit (PSU)



- Faults in the power devices are considered
- Faults in the PSU boost cell are also considered

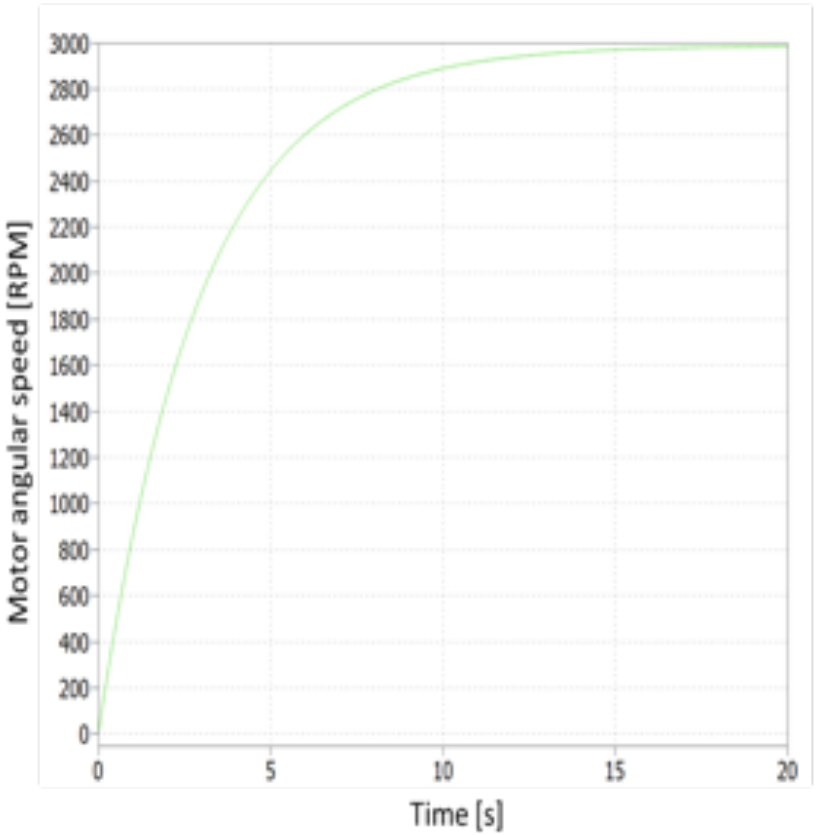
DUT	# Catastrophic faults considered	# Critical faults identified
STTH12S06 diode	4	4
STGF19NC60 IGBT	31	2
PCB boost cell	9	4
TOTAL	44	10

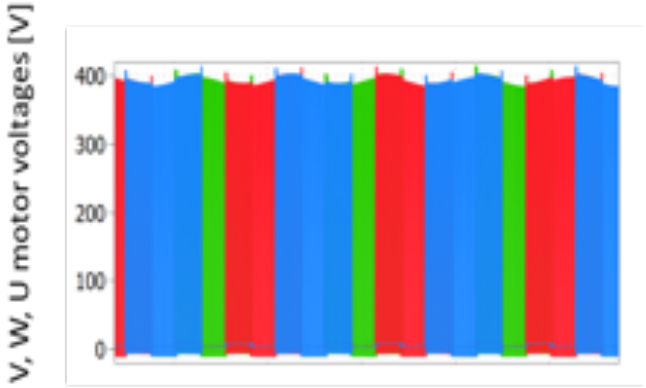
PSU boost cell faults considered

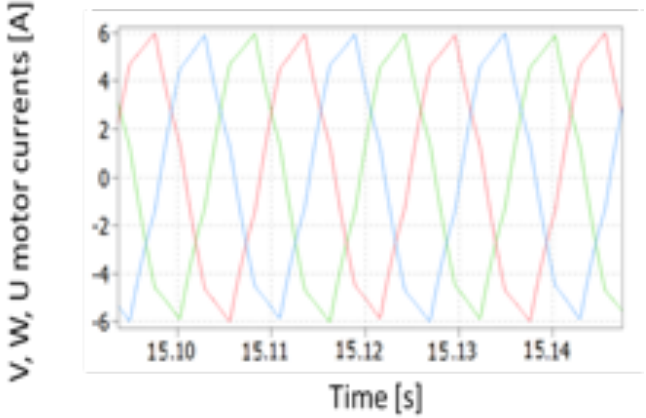


- The three-phase motor reaches the required angular speed (3000 RPM) in about 15 seconds
- The three-phase motor voltage is about 400 V
- The three-phase motor current has a sinusoidal trend with a peak of 6 A
- The cyber-physical system complies with the design specifications

Cyber-physical system behavior in fault-free scenario

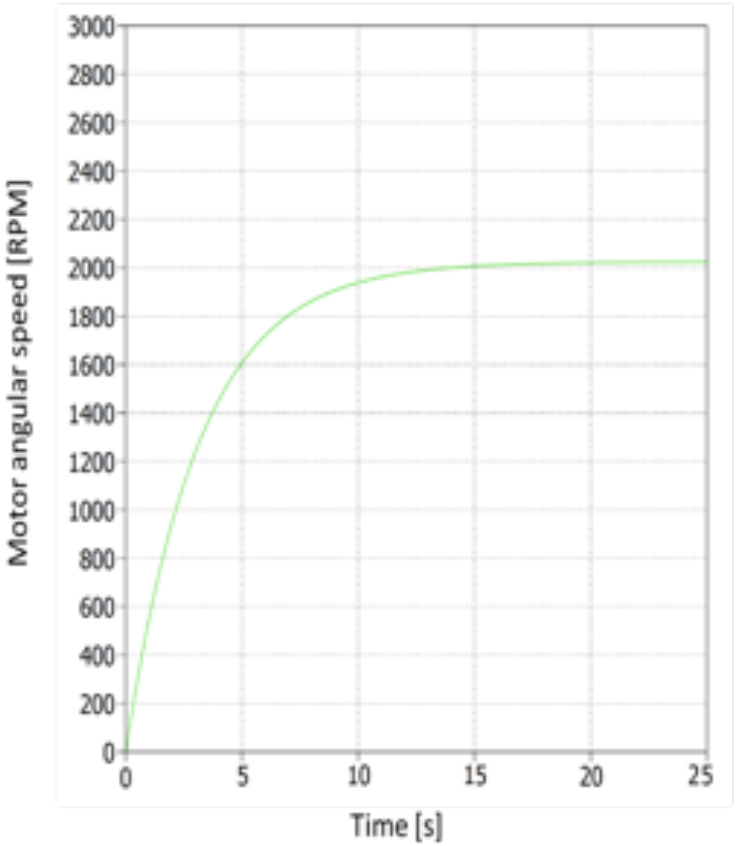


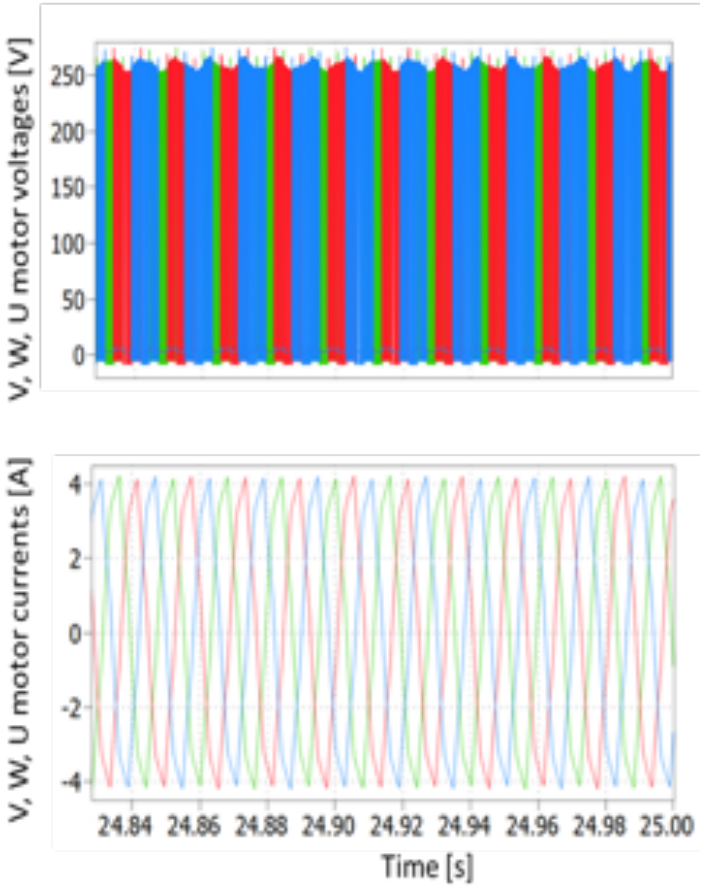




- The three-phase motor does not reach the required angular speed
- The three-phase motor voltage is about 250 V
- The three-phase motor current has a sinusoidal trend with a peak of 4 A
- The cyber-physical system does not comply with the design specifications

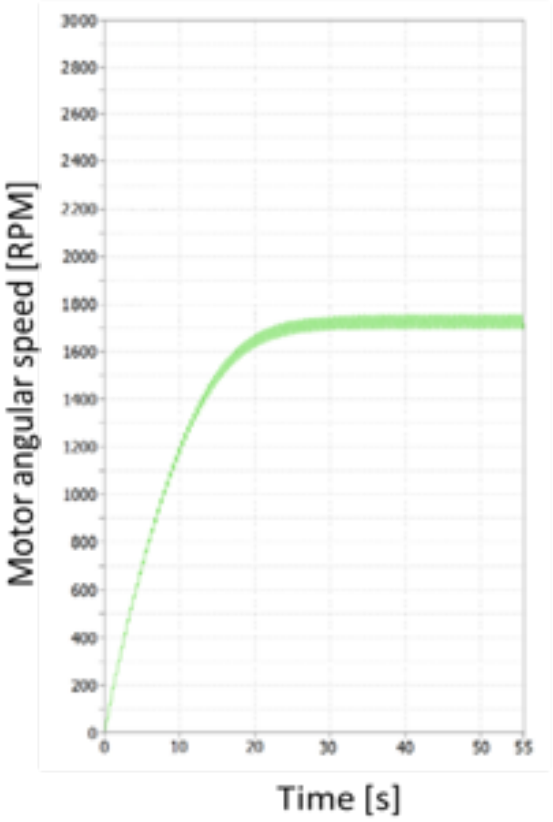
Cyber-physical system behavior affected by a fault in a PSU diode

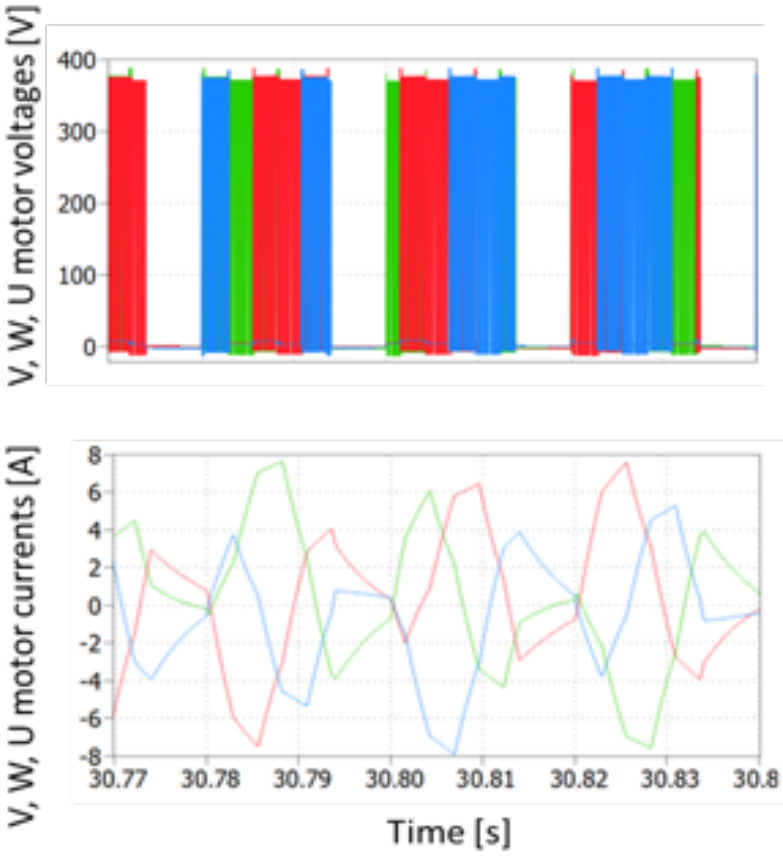




- The three-phase motor does not reach the required angular speed
- The three-phase motor voltage is about 370 V
- The three-phase motor current has not the required sinusoidal trend
- The cyber-physical system does not comply with the design specifications

Cyber-physical system behavior affected by a faults in a PSU boost cell





- A possible methodology to study the impact of possible catastrophic faults present in power devices has been proposed
- The catastrophic fault effect on the whole cyber-physical systems behavior must be analyzed in order to identify the power device critical faults
- The proposed approach is based on multilevel simulations that involve behavioral and structural models of the cyber-physical subsystems
- The multilevel simulation is a good trade-off between the time required for the different fault simulations and the accuracy needed to model the low-level faults considered
- The proposed approach is generic because it is possible to simulate different types of cyber-physical systems by using or developing the appropriate low- and high-level models
- The proposed approach can be adopted resorting to modern and versatile EDA simulation tools (such as SIMULINK/MATLAB)

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6. **CONCLUSIONS**

THESIS CONCLUSIONS

- A possible approach for automatically and systematically generate the power device fault list is proposed
- The fault list is composed of a countable set of faults generated with precise and univocal rules independent on the power device under test
- A possible approach to assess the effectiveness of a test method in a quantitative way (i.e. computing a FC figure) for a power device is proposed
- The proposed approach highlights the limitations, weaknesses and advantages of each test method
- The proposed methodology is helpful for a reliability engineer to predict the cost of the test (in terms of test execution time and of needed resources)

THESIS CONCLUSIONS

- The reliability of the power devices strongly depends to the device junction temperature
- High junction temperature activates different breakdown and ageing mechanisms in the power devices
- The cooling solution used for reducing the devices junction temperature must be adequately tested
- A test method for checking the assembly of the heatsinks is proposed and assessed
- A thermal fault model standard is considered
- The effectiveness of the thermal test procedure is assessed by injecting the thermal faults in the thermal model of the cooling system

THESIS CONCLUSIONS

- A possible approach to study the effect of the power devices catastrophic faults on the cyber-physical system behavior has been proposed
- The proposed approach allows for a comprehensive, systematic and automated FMECA analysis of the power device faults in order to identified the critical faults
- The multilevel simulation involves the behavioral and electrical models of the subsystems present in the cyber-physical systems
- The multilevel simulation is a trade-off between the simulation time and the simulation accuracy required for simulating the power device catastrophic faults
- The proposed approach can be used to assess the effectiveness of the fault mitigation strategy introduced

QUOTES

Google Scholar

Davide Piumatti
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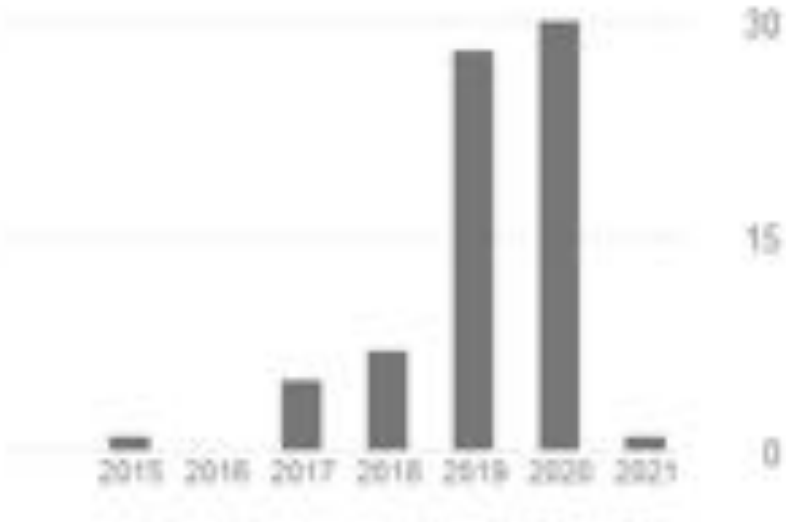
testing digital electronics computers programming analog power electronics

	All	From 2016
Quotes	74	71
H-index	5	5
i10-index	2	2



Analog Test, Thermal Test and FMECA Papers	
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THANKS FOR YOUR ATTENTION

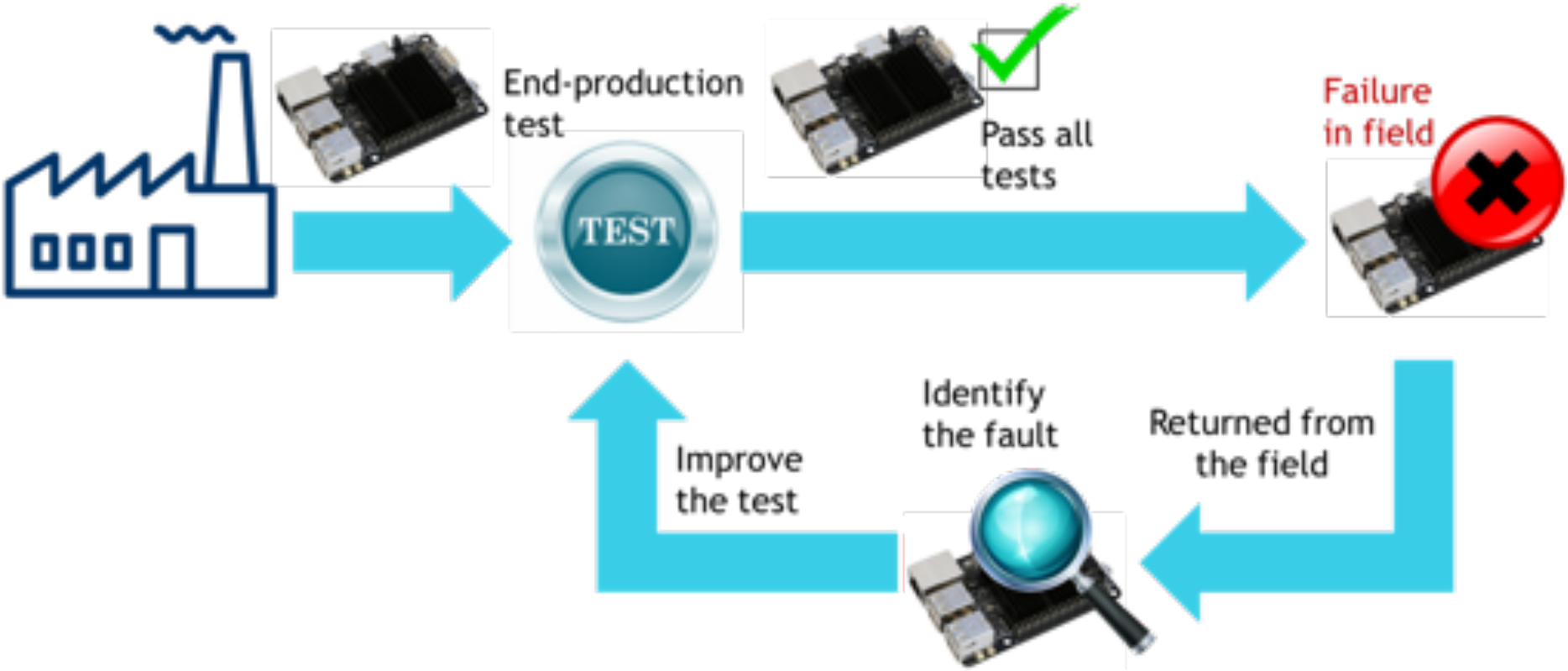
ANY QUESTIONS ?

"The progressive development of man is vitally dependent on the inventions."
Nikola Tesla

ASSESS THE EFFECTIVENESS OF A TEST PROCEDURE

- Currently, the effectiveness of a test procedure is assessed in a qualitative way, considering the direct experience of the test engineers or considering the defective products returned from the field

- The effectiveness of the tests is assessed without applying a well-defined fault model



TESTING

END-OF-MANUFACTORING TEST

- The tests are performed at the end of the application production
- The aim is to verify that the manufactured product correctly works after the factory assembly phases
- The product is tested using an Automatic Test Equipment (ATE)
- In general, the product does not pass the test because a device is defected
- A good test process must eliminate all defected products before they reach the final user

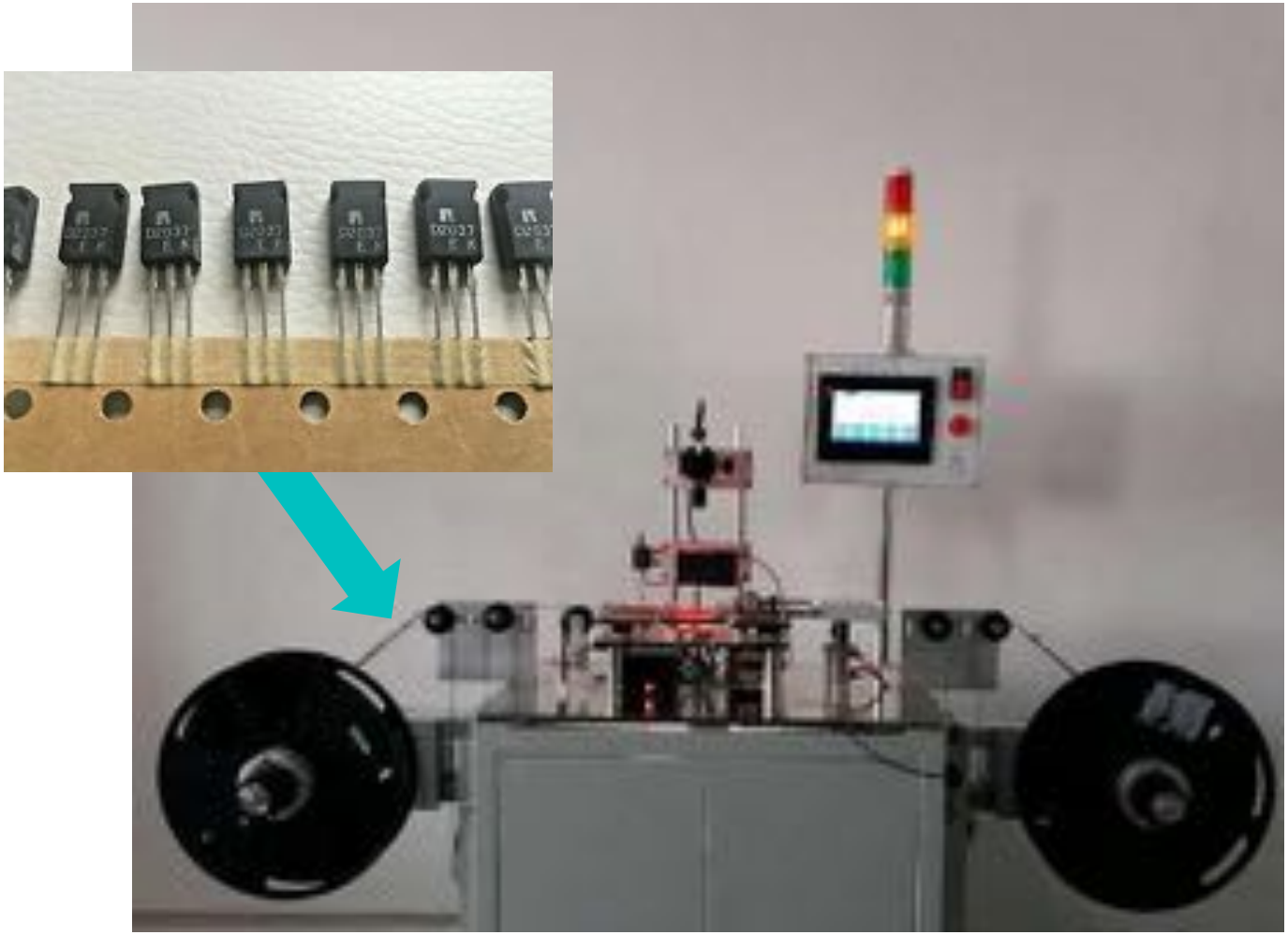
IN-FIELD TEST

- The test are periodically performed in-field during the mission of the production
- The aim is to verify that the product correctly works over-time
- The test requires to be run by placing the product in a particular test configuration
- The test must not influence the behavior of the product in-field during its mission
- A good test process must detect all possible occurrent faults

Regardless of the test strategy adopted, it is necessary to assess the effectiveness of the test strategies adopted

INCOMING INSPECTION TEST

- It is performed on a single device
- The device under test is disconnected from the PCB
- Some test stimuli are applied to the device under test
- The device stimuli response is measured and compared with the expected one



IN-CIRCUIT TEST

- The device under test is assembled on a Printed Circuit Board (PCB)
- It is performed using an Automatic Test Equipment (ATE)
- The ATE directly contact the device under test and applies some test stimuli
- The ATE measures the stimuli response on the device under test
- Guard probes can be required

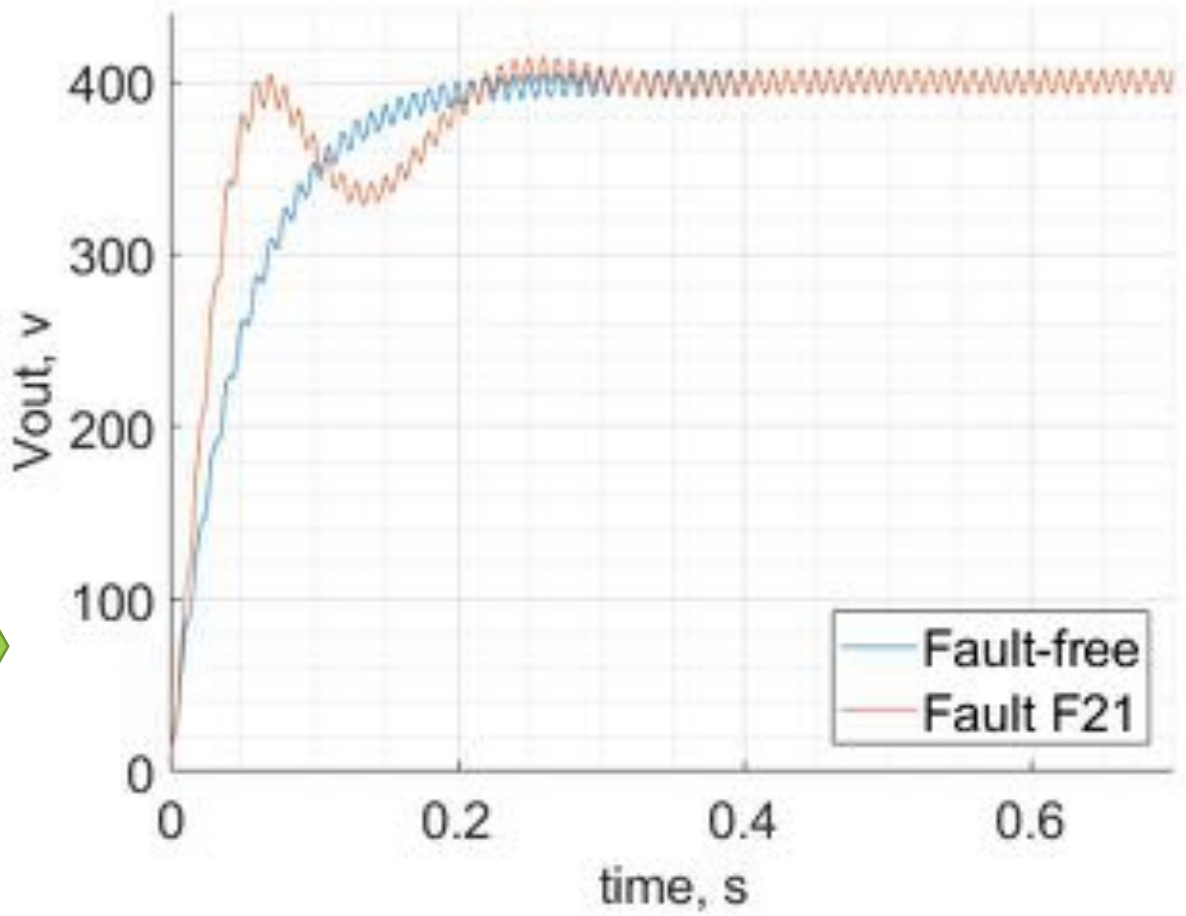
FUNCTIONAL TEST

- The PCB test is performed with respect to its design specifications
- Only the input/output PCB interfaces are used
- Some functional test stimuli are applied to the PCB input port
- In steady state, the stimuli response are measured on the PCB output port

FUNCTIONAL TIMELY ENHANCED TEST

- It is similar to the classic functional test
- The transient stimuli response is also analyzed (in addition to the steady-state stimuli response)
- The ATE must allow this analysis

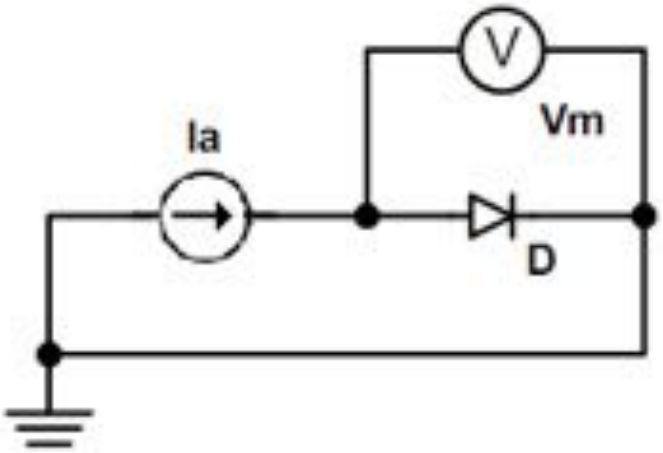
- The simulation is related to a catastrophic fault in the IGBT of the high-voltage PSU



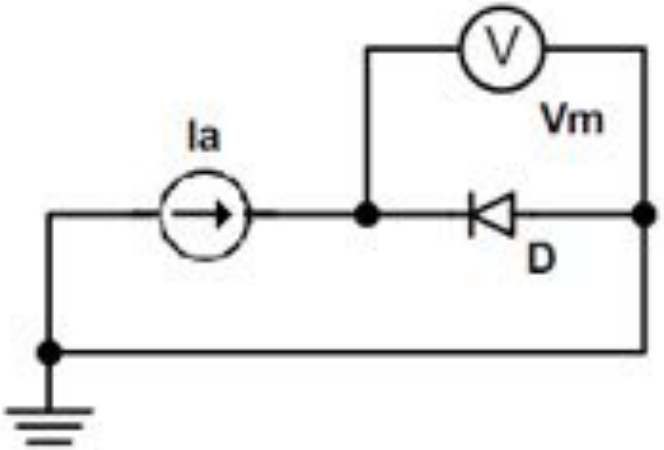
FUNCTIONAL OBSERVABILITY ENHANCED TEST

- It is similar to the classic functional test
- Some functional test stimuli are applied to the PCB input port
- In steady state, the stimuli response are directly measured on the device under test
- This approach (called hybrid) combines the in-circuit approach with the functional approach
- The ATE must allow the hybrid approach

DIODE INCOMING INSPECTION TEST PROCEDURE



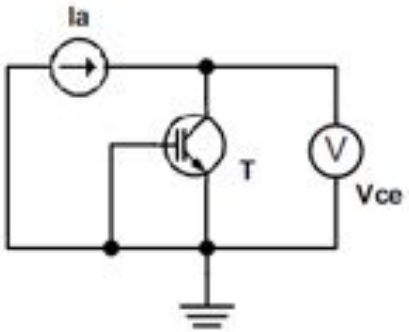
1) PN junction test directly biased



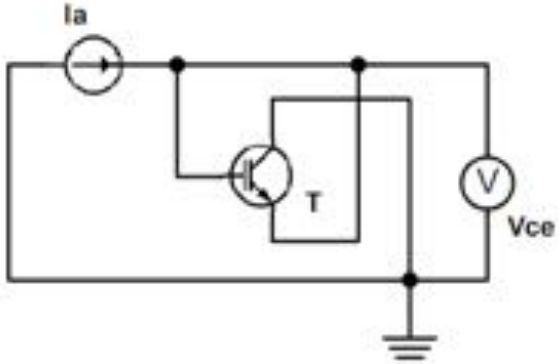
2) PN junction test revers biased

- This test procedure is proposed by Fluke company

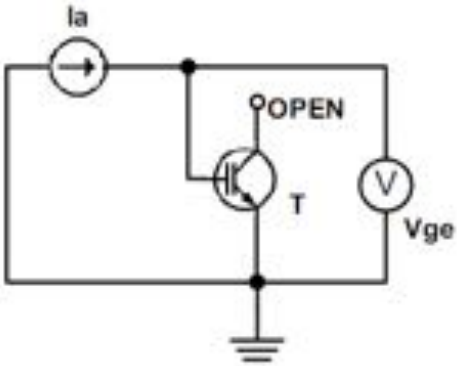
IGBT INCOMING INSPECTION TEST PROCEDURE



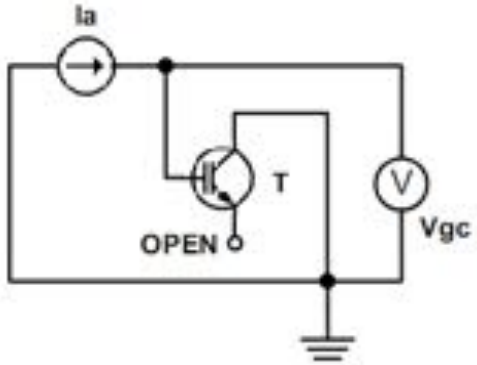
1) PN junction test polarized inversely



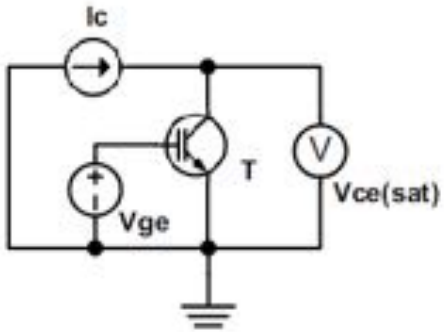
2) PN junction test directly biased



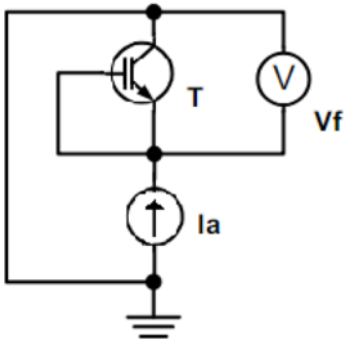
3) Gate-emitter impedance test



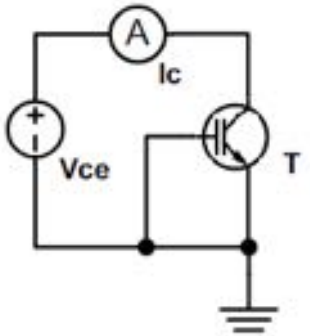
4) Gate-collector impedance test



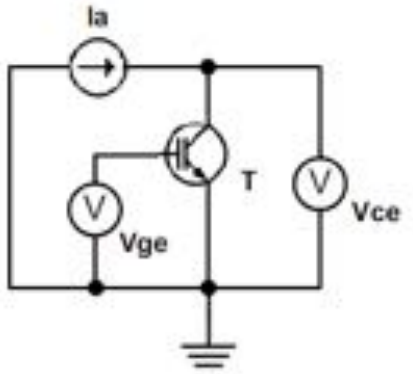
5) Vce(sat) test



6) Antiparallel diode (Vf test)



7) Ices test (blocking device)



8) Vge(th) test

- This test procedure is proposed by Galco company

CATASTROPHIC FAULT LIST GENERATION

- Three different types of switches can be inserted in the equivalent electrical model of the power device

  1) switches to be introduced in **series** to the model components
  2) those to be introduced in **parallel** to the model components
  3) "**topological**" switches, which model possible shorts between the model lines

- The algorithm consists of the following steps

  1) In the equivalent electrical model, **the ideal and parasitic components must first be identified**

  2) The **serial electrical switches are inserted** in series to each component of the circuit

     Two switches placed in series in the same electrical branch can be replaced by a single equivalent switch
     The switches that disconnect only the parasitic components are not considered

  3) The **parallel electrical switches are inserted** in parallel to each component of the circuit

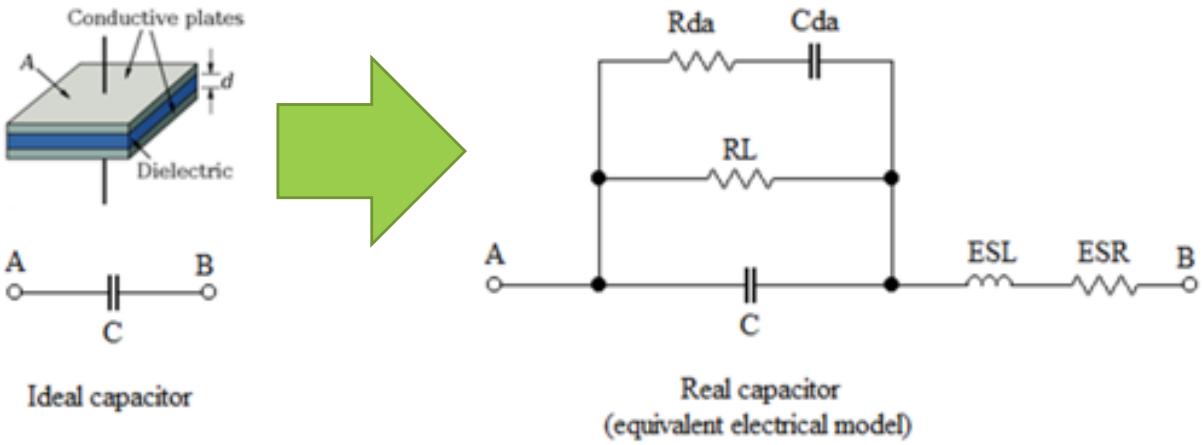
     Two switches placed in parallel to the same component are replaced by a single equivalent switch
     The switches that short-circuit only the parasitic components are not considered

  4) To model the topological faults, **a graph representing the circuit connections is considered**

     The vertices are the nodes of the electrical network, while the components are the edges
     The graph is obtained collapsing the adjacent electrical nodes and collapsing the edges that connect the same nodes
     A "topological" fault is considered for each missing edge in the graph
     The switches that short-circuit only the parasitic components are not considered

CATASTROPHIC FAULT LIST GENERATION - EXAMPLE

1) In the equivalent electrical model, **the ideal and parasitic components must first be identified**

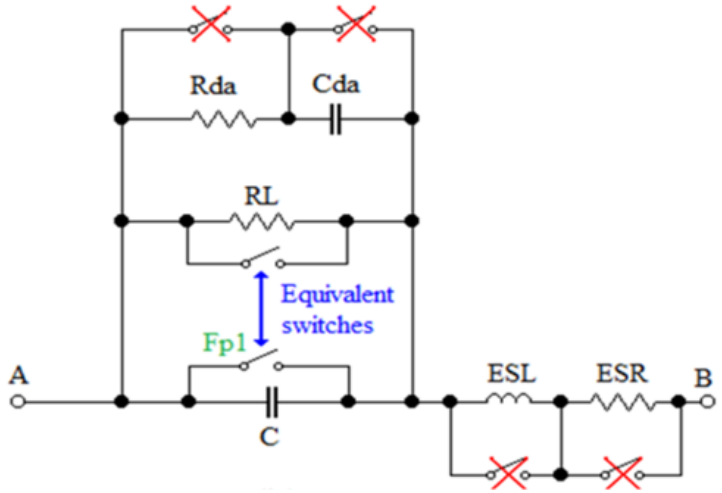


Component	Description	Parasitic/ ideal
Rda	Dielectric absorption	Parasitic
Cda	Dielectric absorption	Parasitic
RL	Dielectric electrical permeability	Parasitic
C	nominal capacitance	ideal
ESL	Equivalent series inductance	Parasitic
ESR	equivalent series resistance	Parasitic

2) The **serial electrical switches are inserted** in series to each component of the circuit

CATASTROPHIC FAULT LIST GENERATION - EXAMPLE

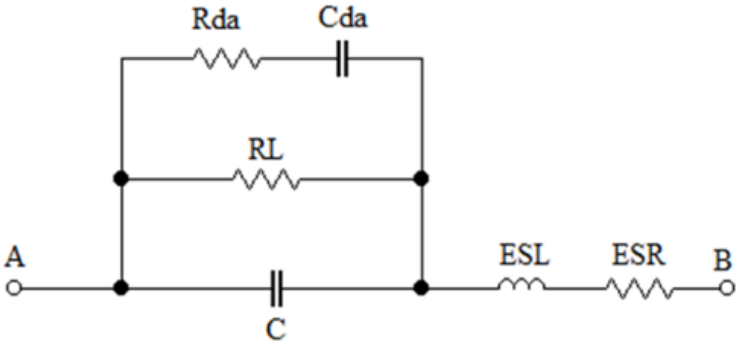
3) The **parallel electrical switches are inserted** in parallel to each component of the circuit

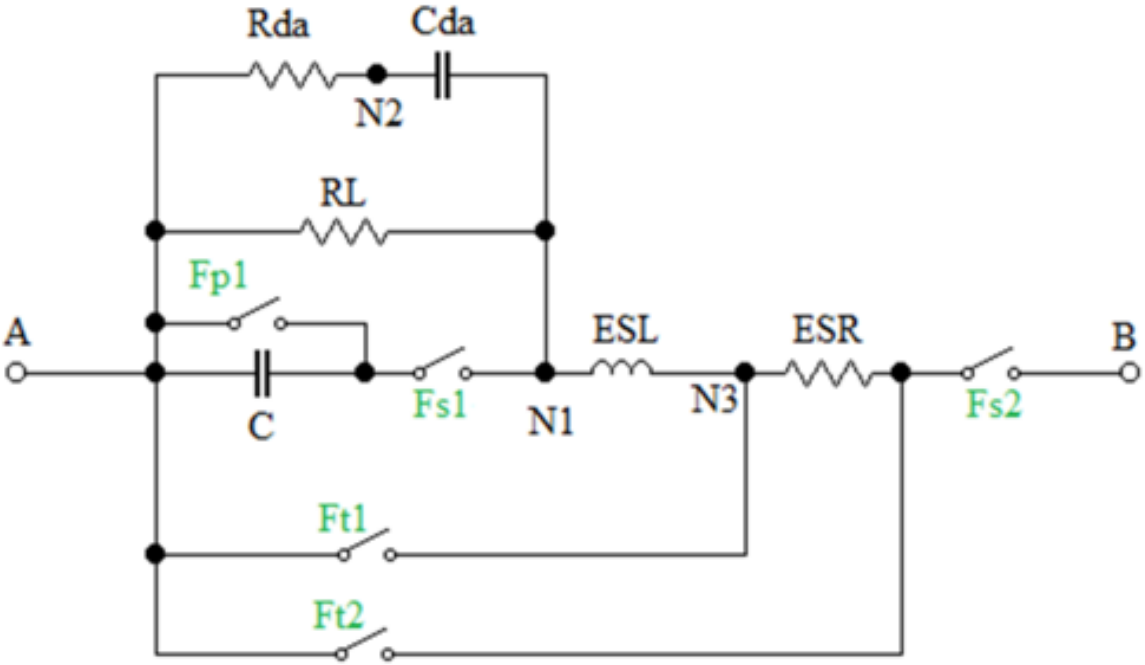


4) To model the topological faults, **a graph representing the circuit connections is considered**

CATASTROPHIC FAULT LIST GENERATION - EXAMPLE

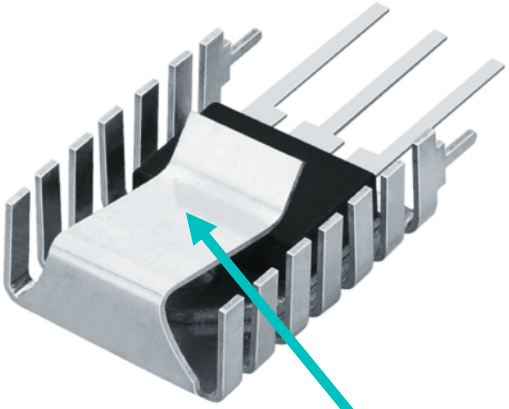
5) Equivalent electrical model of the capacitor with the switches modeling possible catastrophic faults

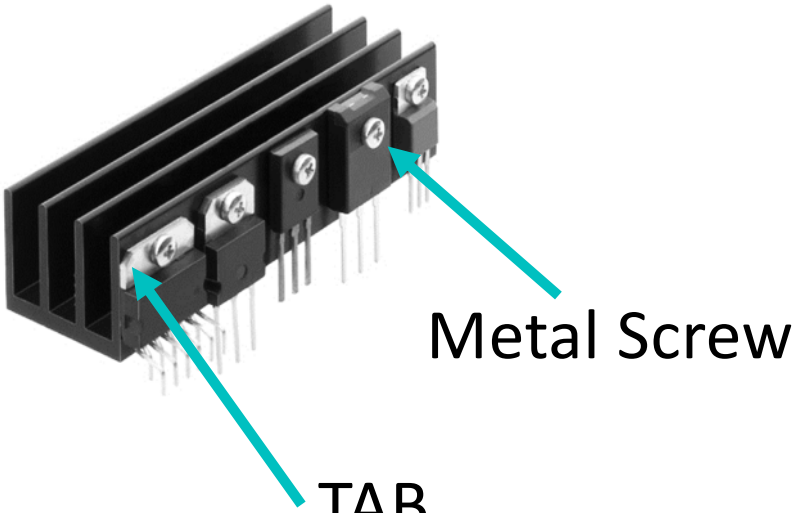




Catastrophic faults	
Serial	2
Parallel	1
Topological	2
TOTAL	**5**

HEATSINK ASSEMBLY

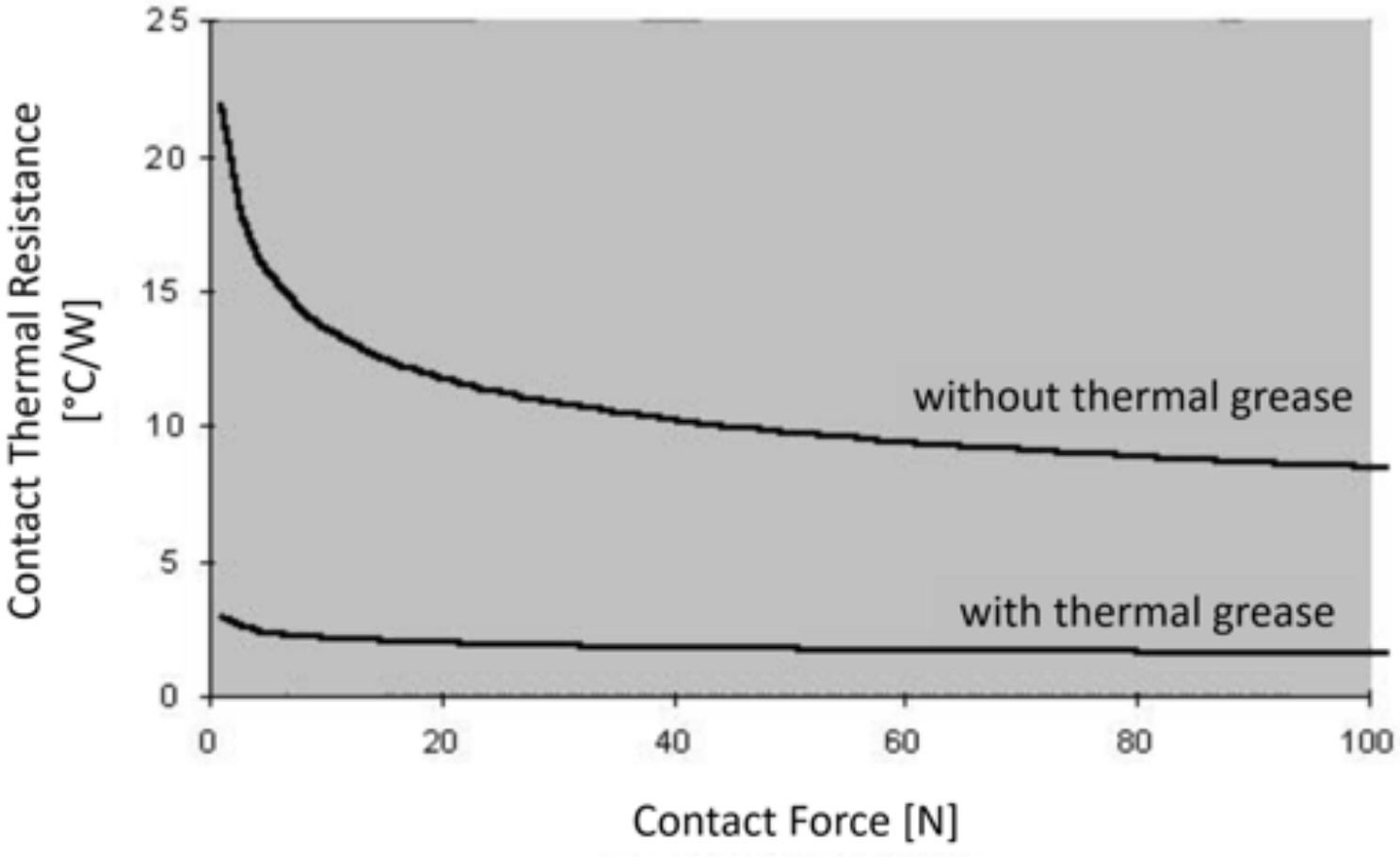




HEATSINK ASSEMBLY - THERMAL CONTACT RESISTANCE

- The value of the thermal contact resistance depends on the anchoring force that the heatsink exerts on the power device

- Figure extracted from the International Rectifier Application Note AN-997

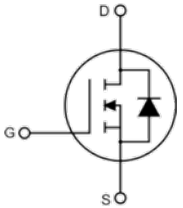


TEMPERATURE-SENSITIVE ELECTRICAL PARAMETERS (TSEP)

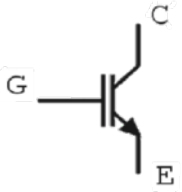
- The power device junction temperature can be estimated by means of some electrical parameters sensitive to the junction temperature
- In general, voltages and currents on the power device are measured
- A TSEP characterization phase of the power device is necessary
- The TSEP relationship can be provided by the manufacturer or it can be experimentally obtained

DIODE 

$V_{AK,ON}$ (Tj)

MOSFET 

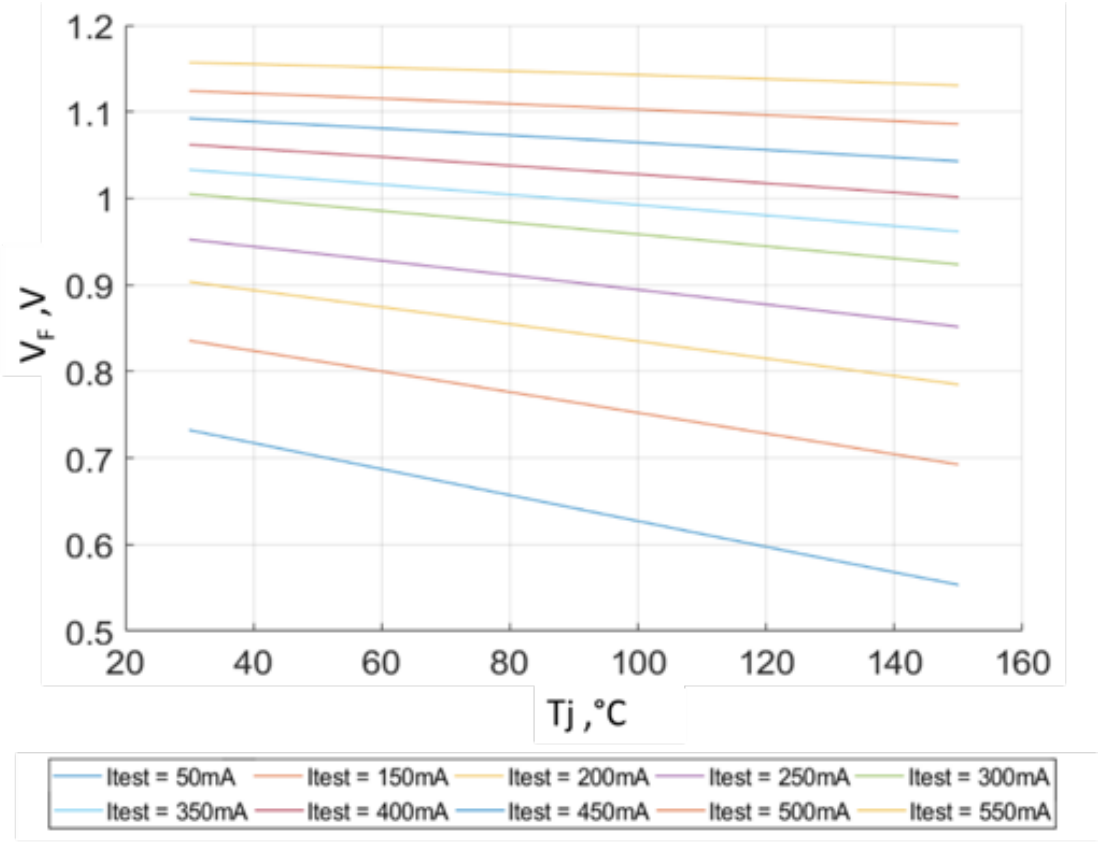
$R_{DS,ON}$ (Tj)

IGBT 

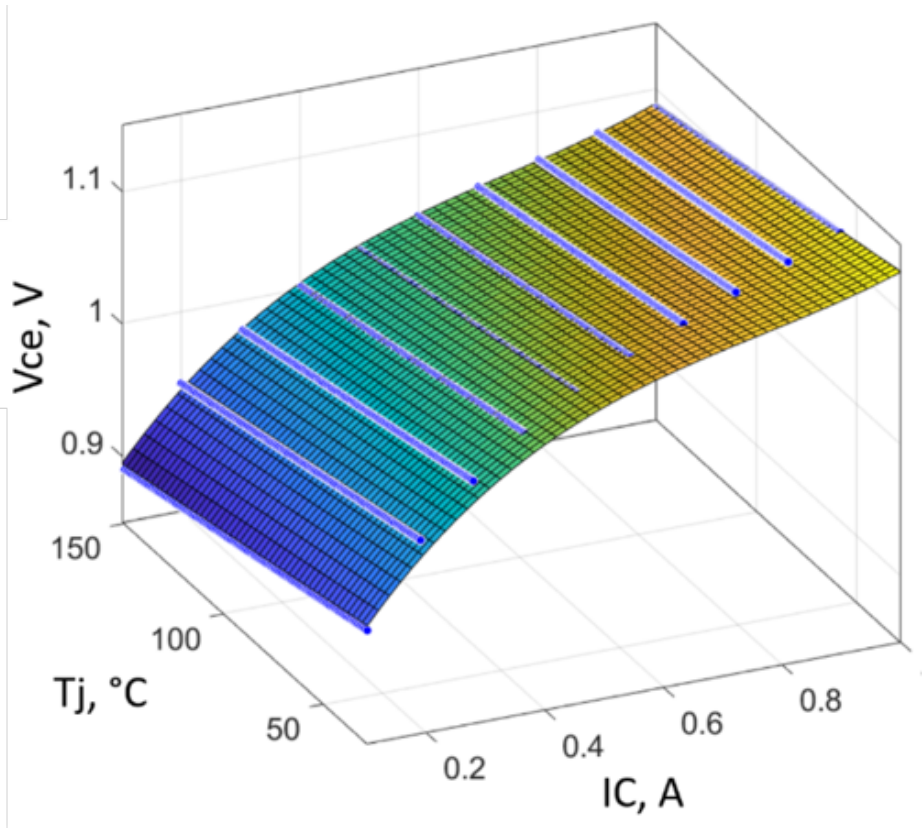
$V_{CE,ON}$ (Tj, Ic)

TEMPERATURE-SENSITIVE ELECTRICAL PARAMETERS (TSEP)

TSEP DIODE

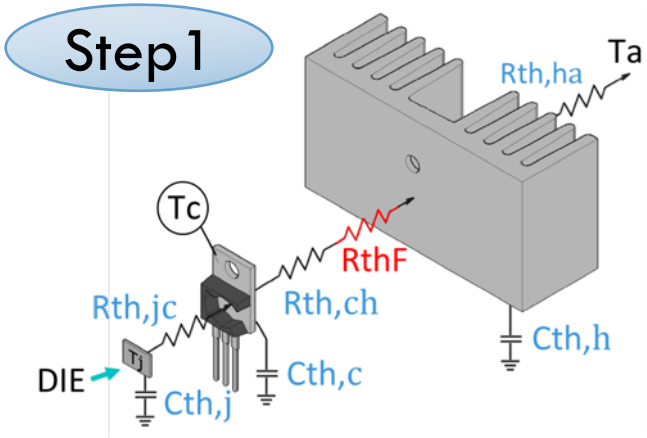


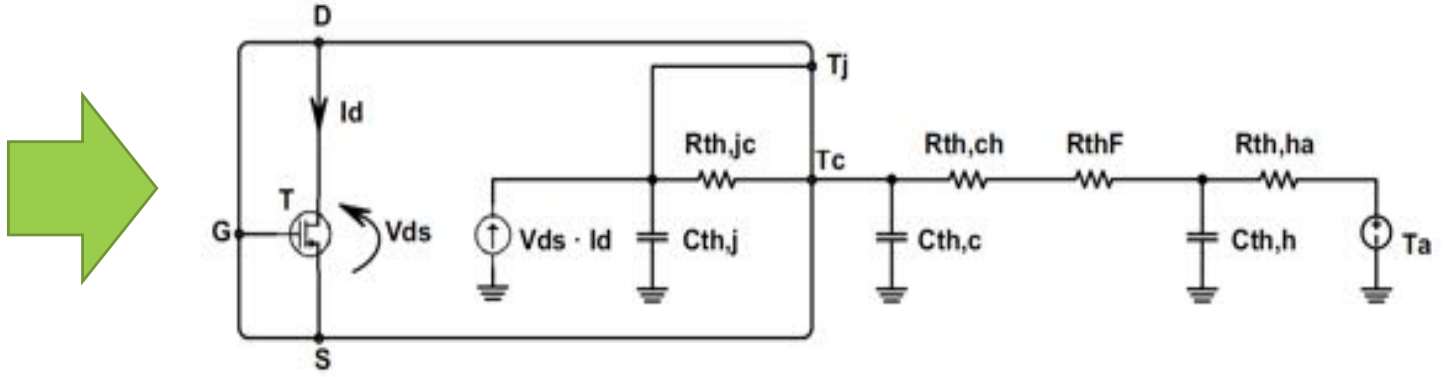
TSEP IGBT



THERMAL FAULT GENERATION FLOW

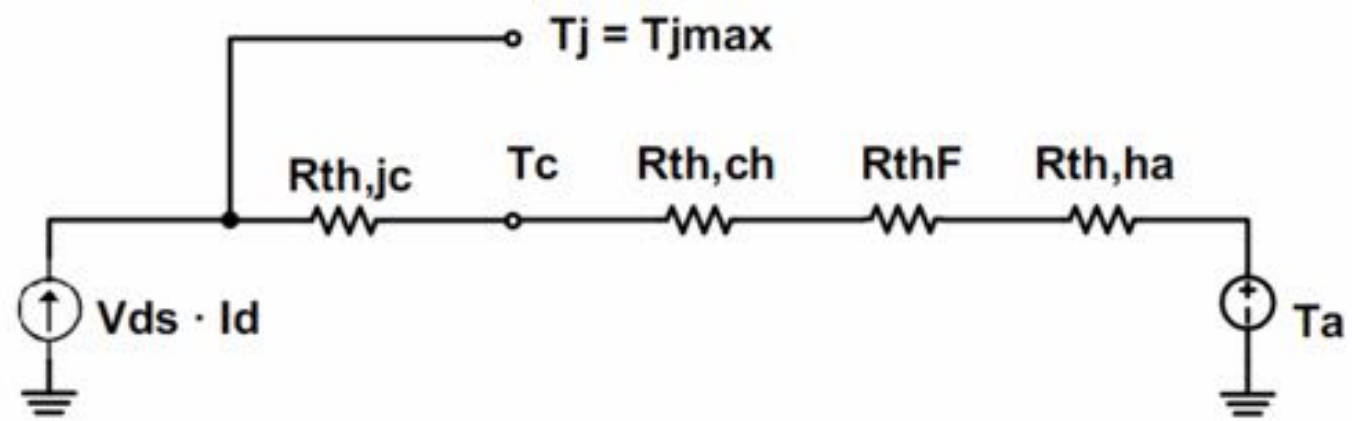
Step1





Step2

- The TJMAX value is imposed with the thermal network in steady-state
- The value of the RthF can be calculated resolving the thermal network with the superposition theorem



$$RhtF = \frac{Tjmax - Ta}{Vds \cdot Id} - Rth,jc - Rth,ch - Rth,ha$$

IN-CIRCUIT THERMAL TEST

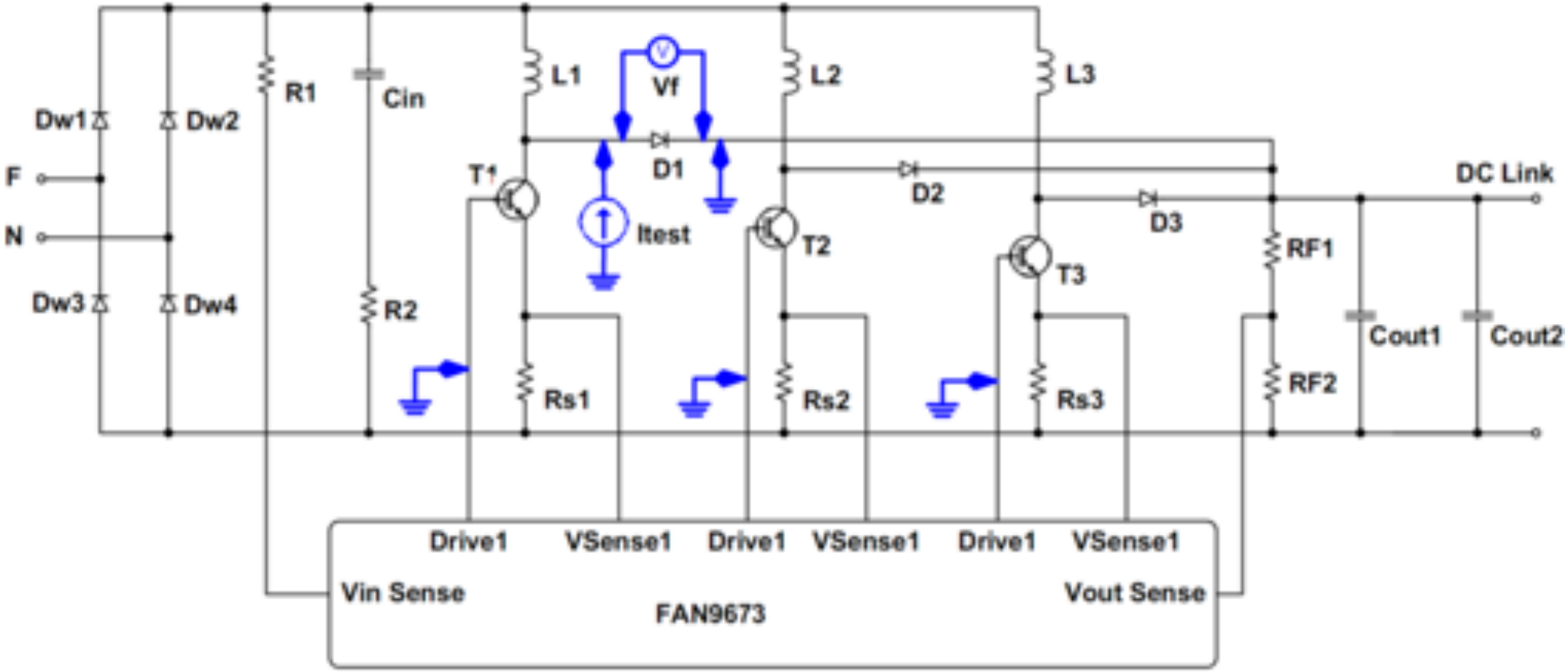
- The thermal test is performed with the following steps

1) Using an automatic test equipment, a test stimulus is applied to the power device with the aim of heating it
2) In steady state, the current flowing through the device and the voltage drop across the power device are measured
3) Using the temperature-sensitive electrical parameters, the junction temperature (Tj) inside the power device is estimated
4) The ambient temperature (Ta) is measured
5) The ambient junction thermal resistance (Rth,ja) is calculated with the following equation

$$R_{th,ja} = \frac{T_j - T_a}{P_M}$$

6) If the thermal resistance Rth,ja exceeds the expected value, the proposed approach detects a defect in the heatsink assembly

IN-CIRCUIT THERMAL TEST DIODE PROCEDURE



- The Itest is a direct current; therefore, the inductors are short circuits. The diodes are in parallel.

EXPERIMENTAL RESULTS WITH THE HEATSINK INCORRECTLY ASSEMBLED

- Experiments performed with a SPP07N60 MOSFET
- Seven different heatsink assembly configurations were considered
- The ambient junction thermal resistance (Rth,ja) is measured with the proposed approach
- The TSEP considered is the RDS,on of the MOSFET